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A Microdevice in a Submicron CMOS for Closed-Loop Deep-Brain Stimulation (CLDBS)

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Abstract: Deep-brain stimulation (DBS) is a highly effective and safe medical treatment that improves the lives of patients with a wide range of neurological and psychiatric diseases. It has been established as a first-line tool in the treatment of these conditions for the past two decades. Closed-loop deep-brain stimulation (CLDBS) advances this tool further by automatically adjusting the stimulation parameters in real time based on the brain's response. In this context, this paper presents a low-noise amplifier (LNA) and a neurostimulator circuit fabricated using the low-power/low-voltage 65 nm CMOS process from TSMC. The circuits are specifically designed for implantable applications. To achieve the best tradeoff between input-referred noise and power consumption, metaheuristic algorithms were employed to determine and optimize the dimensions of the LNA devices during the design phase. Measurement results showed that the LNA had a gain of 41.2 dB; a 3 dB bandwidth spanning over three decades, from 1.5 Hz to 11.5 kHz; a power consumption of 5.9 µW; and an input-referred noise of 3.45 μV_{RMS}, from 200 Hz to 11.5 kHz. The neurostimulator circuit is a programmable Howland current pump. Measurements have shown its capability to generate currents with arbitrary shapes and ranging from −325 µA to +318 µA. Simulations indicated a quiescent power consumption of 0.13 µW, with zero neurostimulation current. Both the LNA and the neurostimulator circuits are supplied with a 1.2 V voltage and occupy a microdevice area of 145 µm × 311 µm and 88 µm × 89 µm, respectively, making them suitable for implantation in applications involving closed-loop deep-brain stimulation.

Keywords: closed-loop deep-brain stimulation; low-noise amplifier; neurostimulation; implantable devices

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1. Introduction

Deep-brain stimulation (DBS) is a surgical procedure that involves the implantation of a medical device called a neurostimulator (often referred to as a brain pacemaker) that sends mild impulses to specific areas of the brain through implanted electrodes [1]. The electrical currents used in DBS are very low, typically in the range of microamperes, and they are applied to strategic points, primarily located deep within the brain tissue. This procedure involves inserting implantable tips, with electrode rings at the ends, into specific points in

the thalamus, the subthalamic region, and the globus pallidus, among other structures. The electrodes are connected to the neurostimulator via extension cables containing metallic wires [2]. The neurostimulator is a device with dimensions no larger than that of a matchbox and includes an attached battery to provide power for its operation [3]. The first use of the DBS technique dates back to 1997, when the American FDA, for the treatment of Parkinson's disease [4], granted authorization for its use. Since then, the DBS has become a first-line therapy option for relieving symptoms associated with neurological and movement disorders that are unresponsive to other therapies, namely, chronic pain, dystonia, Parkinson's disease, Tourette's syndrome, essential tremor, obsessive–compulsive disorder, and morbid obesity [4].

There are two paradigms for classifying DBS, namely, open-loop DBS (also known as conventional DBS) and closed-loop DBS (also known as adaptive DBS or CLDBS) [3,5,6]. In the case of open-loop DBS, a neurologist manually adjusts the stimulation parameters every 3–12 months after implantation. On the other hand, for CLDBS, the adjustment of stimulation parameters is performed automatically based on some measured biomarkers [3,6]. Biomarkers are acquired signals, and they can have different natures, namely, bioelectrical, biochemical, and psychological, among others [3,6]. Biomarkers are essential indicators in CLDBS because, based on the disease to be treated, they help to adaptively reconfigure the signals used in neurostimulation [3,6].

Advances in microelectronics are paving the way for the simultaneous acquisition of multiple types of biopotentials using a single device, enhancing CLDBS. The development of the CMOS blocks presented in this paper was motivated by this capability.

Figure 1 illustrates the block diagram of a system designed for applications in CLDBS. The diagram comprises three main modules: the power management module, the RF communications module, and the CMOS microdevice, which serves as the front-end circuit. The CMOS microdevice is responsible, on one hand, for acquiring neuronal signals, filtering them, and converting them to a digital format. Furthermore, it is responsible for applying neuronal stimuli according to received instructions. Of particular significance within the CMOS microdevice are two pivotal circuits: the low-noise amplifier (LNA) and the neurostimulator, depicted respectively in yellow and green colors in the block diagram.

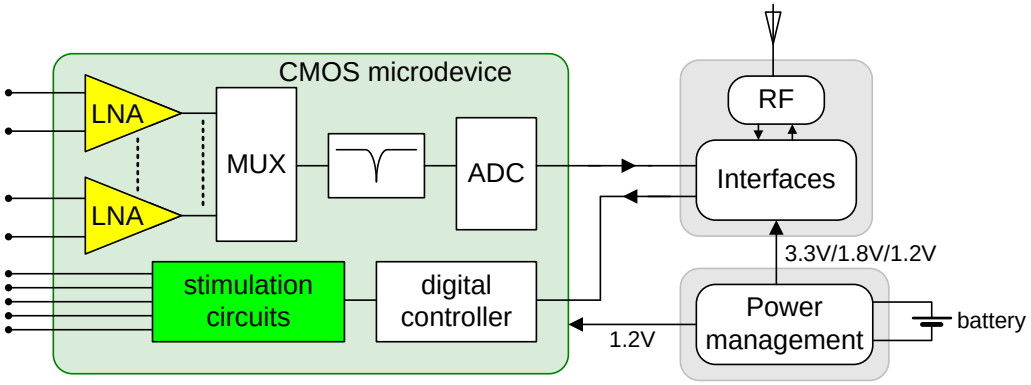


Figure 1. Block diagram of a system for applications in CLBDS. The system is composed of a power management module, a communications module, and the CMOS microdevice, containing the acquisition blocks, the neurostimulator, and the control block. The proposed circuits, LNA, and the neurostimulator are filled with the yellow and green colors, respectively.

In this paper, we present an LNA and a neurostimulator circuit designed specifically for implantable applications. The LNA is based on a simple differential amplifier configuration, and its design and optimization were accomplished through the application of metaheuristic algorithms. The circuit can capture local field potentials (LPFs), characterized by frequencies below 200 Hz and amplitudes under 5 mV, but it is primarily optimized for action potentials (APs), with frequencies ranging from 200 Hz to 7 kHz and amplitudes under 200 µV [7]. The neurostimulator circuit was designed to generate arbitrary current

pulses with a biphasic shape. Both circuits were implemented in a 65 nm CMOS process. The rest of this paper is organized as follows: Section 2 presents the circuit designs, Section 3 details the experimental results, Section 4 provides comparisons between our circuits and others found in the literature, and, finally, Section 5 concludes the paper.

2. Design

In this section, the LNA and the neurostimulator designs are presented.

2.1. Low-Noise Amplifier (LNA)

Signals at the input of an LNA present a variety of challenges, such as low amplitudes, on the order of microvolts, and low frequencies, close to 0 Hz. The amplifiers for neural recordings, found in the literature, typically exhibit a mid-band gain of 40 dB, with bandwidths ranging from sub-hertz to a few kilohertz or even a few dozen kilohertz [8–13].

LNAs are usually implemented using a high-gain amplifier and capacitive feedback, where capacitors are employed to set the gain and achieve a DC offset rejection [7,14]. Figure 2a shows a schematic of this configuration. It comprises a differential amplifier, two pairs of capacitors, C_1 and C_2, and a pair of large pseudo-resistors R_2. The function of the resistors, together with the capacitors, is to generate a low cutoff frequency.

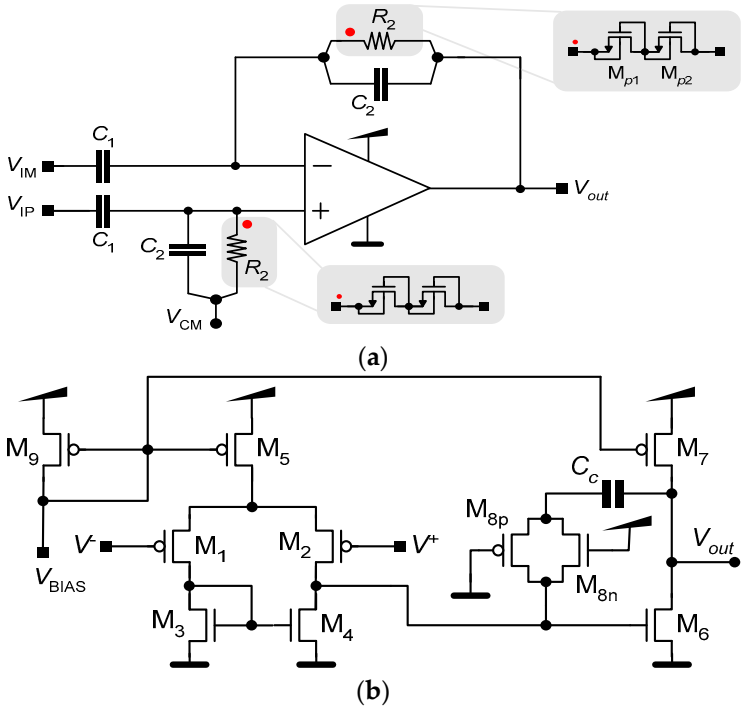


Figure 2. Schematics of (**a**) an LNA and (**b**) the operational amplifier. The red dots on (**a**) indicate how the pseudo-resistors connects to the operational amplifier.

Instead of differential amplifiers, a single-input CMOS inverter can be used for amplification [7]. An LNA with a CMOS inverter has half the number of transistors in the amplifier compared to the input stage of a differential amplifier and, therefore, introduces approximately half the amount of power noise. However, they will exhibit high sensitivity to supply voltage variations and poor linearity [7,9].

A typical LNA implementation employs operational transconductance amplifiers (OTAs). Various OTA topologies, including both single and differential outputs, have been employed. A symmetrical OTA was utilized in [10], while a folded cascade was employed in [15]. Additionally, to suppress voltage offset and 1/f flicker noise, switched-capacitor techniques are often considered [7,14].

In our approach, we employ the simple OTA presented in Figure 2b. The OTA has a basic structure with two stages. The first stage is a differential pair that works as the input stage. The second stage is a common source amplifier and provides additional gain to the input stage, thereby increasing the total gain of the operational amplifier. The PMOS (M_{8p}) and the NMOS (M_{8n}) act as a resistor in series with the capacitor (C_c), creating a pole and ensuring that the operational amplifier is unconditionally stable. The transfer function of the LNA is given as follows:

$$\begin{aligned} A_f(s) = \frac{V_{out}}{V^+ - V^-} &\approx -\frac{ks}{\left(\frac{s}{2\pi f_L}+1\right)\times\left(\frac{s}{2\pi f_H}+1\right)} \\ &= \frac{R_2C_1 s}{(sR_2C_2+1)\times\left(s\frac{A_{\text{mband}}}{2\pi f_p A_0}+1\right)} \end{aligned} \quad (1)$$

where $k = R_2C_1$, $A_{\text{mband}} = (C_1 + C_2)/C_2$, $f_L = 1/(2\pi R_2C_2)$, and $f_H = f_pA_0/A_{\text{mband}} = \text{GBW}/A_{\text{mband}}$. The quantities f_p, GBW, and A_0 are, respectively, the dominant pole, the gain × bandwidth product, and the open-loop gain of the operational amplifier. Typically, $f_L << f_H$ and $C_2 << C_1$; then, for medium-frequency operation, i.e., for $f_L <<$ frequency $<< f_H$, the LNA gain is as follows:

$$A_{\text{f}} \approx C_1/C_2 = A_{\text{mband}} \quad (2)$$

Frequencies f_L and f_H are the LNA low and high cutoff frequencies, respectively.

Because capacitances in an integrated circuit are typically on the order of picofarads, the resistor (R_2) must be on the order of teraohms to ensure that the low pole, $f_L = 1/(2\pi R_2C_2)$, of $A_f(s)$ has a value near or lower than 1.0 Hz. The integration of high-value resistors, like R_2, in conventional form is not feasible because of the substantial area they would require. One feasible solution to this challenge involves implementing R_2 through the utilization of pseudo-resistors [16], as depicted in Figure 2b.

To achieve low noise and low power, even using an OTA with a simple configuration, the LNA design in this work was carried out using metaheuristic algorithms, specifically particle swarm and simulated annealing [17,18]. To accomplish this task, a Matlab framework for transistor sizing and circuit optimization, based on metaheuristics, was applied [19,20]. For the calculation of the design score employed in the optimization, the attributes of the operational amplifier and of the complete LNA were taken into consideration. For the operational amplifier, the following attributes were considered: the differential gain (>80 dB), the common-mode rejection rate (CMRR) (>60 dB), the power supply rejection rate (PSRR) (>60 dB), the input common-mode range (from 0.5 V to 0.7 V), the slew rate (>0.08 V/µs), the systematic input voltage offset (<0.1 mV), and the phase margin (between 45° and 60° for an output capacitance of 0.7 pF); for the complete LNA, the considered attributes were as follows: the gain (between 39 dB and 41 dB), the input-referred noise (IRN) (<5.0 μV_{rms}), the low and high cutoff frequencies (6.0 Hz and 7.0 kHz, respectively), the power consumption (minimum), and the area (minimum).

Thermal and biological noises in cortical recordings are approximately 10 μV_{rms} [21,22], so the input-referenced noise of LNAs is expected to be lower than this value. A noise floor as low as 4.0 µVrms is typically pursued by neuronal amplifier designers, but this level is significantly below the levels of thermal and biological noises. Initially, during the design and optimization phase, an input noise of 4.0 µVrms was targeted. However, achieving this level of noise requires a significant amount of power consumption in the utilized process, because of various factors, such as the large gate capacitance of the differential pair transistors, M_1 and M_2. For this reason, in our design, we allowed for a higher input noise while maintaining low power consumption.

It should be noted that technologies with larger minimum dimensions but lower gate capacitances, such as 180 nm technologies, can be advantageously utilized in the design of low-noise LNAs.

Table 1 lists the dimensions of the MOSFETs of the operational amplifier and of the pseudo-resistors, and the values of the capacitors C_1, C_2, and C_c generated by the

sizing/optimization algorithms. The simulated performance parameters of the LNA are a power consumption of 6.16 µW, for a power supply of 1.2 V; low and high cutoff frequencies of 12 Hz and 8.5 kHz, respectively; a gain of 39.9 dB; and input-referred noises (IRNs) of 3.93 μV_{RMS}, from 12 Hz to 200 kHz, of 3.71 μV_{RMS}, from 200 Hz to 8.5 kHz, and 5.4 μV_{RMS}, from 12 Hz to 8.5 kHz. Additionally, the circuit is unconditionally stable for capacitive loads as high as 20 pF.

Table 1. Dimensions of the MOSFETs that comprise the operational amplifier and the pseudo-resistors, and the values of the capacitors C_c, C_1, and C_2 obtained with the optimizer.

MOSFET	**(W/L)**
M_1, M_2	59 µm/0.52 µm
M_3, M_4	25 µm/14.9 µm
M_5	48 µm/2.22 µm
M_6	12.5 µm/14.9 µm
M_7	12 µm/2.22 µm
M_{8n}	1.55 µm/12 µm
M_{8p}	3.1 µm/12 µm
M_9	2 µm/2.22 µm
M_{p1}, M_{p2}	12 µm/0.6 µm
Capacitor	**Total Value**
C_c	7.5 pF
C_1	18.7 pF
C_2	0.18 pF

2.2. Neurostimulator

Neurostimulators must preferably provide current pulses with a biphasic shape because of electrical safety reasons, such as avoiding the accumulation of charges at interfaces between electrodes and ionic species within the neuronal tissue [23]. Figure 3 illustrates four examples of pulse shaping, where the duration (or stimulation times), frequency, amplitudes, and inter-pulse delay of the pulses can be set according to medical requirements. The mean value of these signals is zero in all the examples, thanks to the arbitrary pulse shaping.

To maintain electrical safety, as previously mentioned, the neurostimulator circuit was designed to offer the capability for generating current with a biphasic waveform, which can invert the direction of the charge injection in the neuronal tissue. The phenomenon of nullifying the charge accumulation is called the charge balance [23]. Traditionally, the inversion of the current direction requires a bridge with an H-topology [24], with the disadvantage of requiring four transistors for current inversion, increasing the programming complexity, and access to two different contact points on the electrodes, which are normally unipolar. For these reasons, the circuit responsible for injecting the current into the electrodes is based on the Howland current pump [25]. This circuit is easy to integrate because it uses low resistance values, that is, below 20 kΩ.

Figure 4a shows the schematic of the current pump that implements the neurostimulator. The neurostimulator is composed of an operational amplifier and four resistors {R_1, R_2, R_3, R_4}, all fully implemented using the mask layers of the TSMC 65 nm CMOS process. Figure 4b presents the schematic of the operational amplifier used by the current pump. Table 2 lists the dimensions of the MOSFETs, the values of the operational amplifier's internal capacitances, C_c and C_x, and the values of the current-pump's resistors.

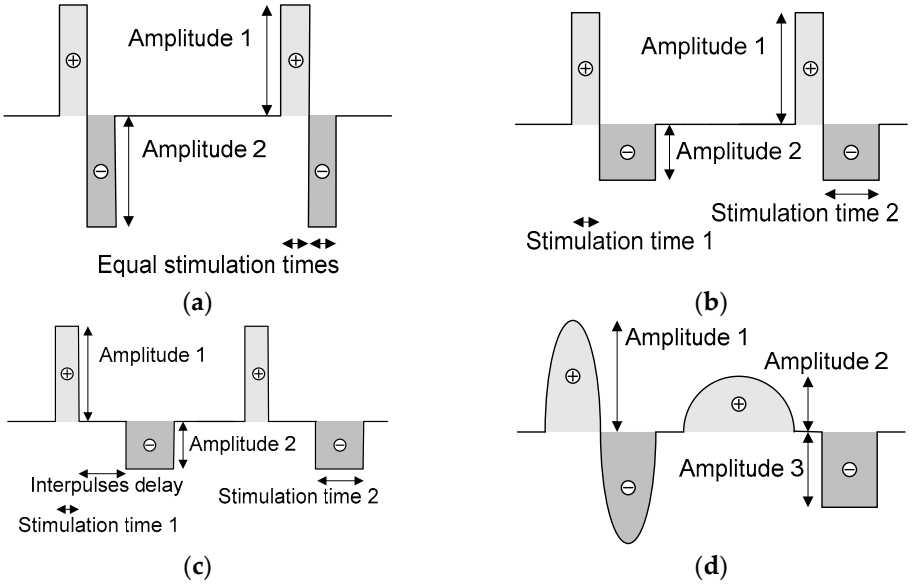


Figure 3. An example of (**a**) a symmetric biphasic pulse shape without an inter-pulse delay and a mean value of zero; two examples of asymmetric biphasic pulse shapes, with (**b**) zero and (**c**) non-zero inter-pulse delays; and an example of (**d**) a signal with an arbitrary shape. All the waves can have a mean value of zero.

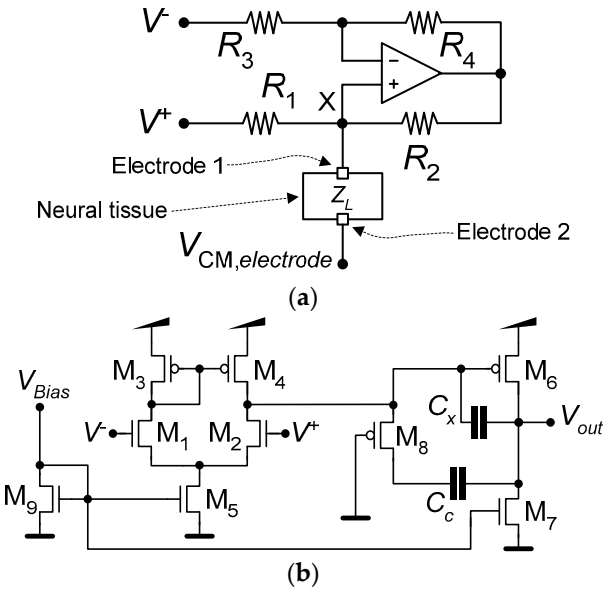


Figure 4. Schematics of (**a**) the current pump that implements the neurostimulator and (**b**) the operational amplifier used by the current pump.

Table 2. Dimensions of the MOSFETs, the capacitors (C_c and C_x) that comprise the operational amplifier, and the resistors of the current pump.

MOSFET	(W/L)
M_1, M_2	14.8 µm/0.24 µm
M_3, M_4	4.68 µm/0.18 µm
M_5	14.4 µm/0.36 µm
M_6	18.72 µm/0.18 µm
M_7	28.8 µm/0.36 µm
M_8	0.51 µm/7.2 µm
M_9	0.80 µm/0.36 µm

Table 2. *Cont.*

Capacitor	Total Value
C_c	2.5 pF
C_x	417.2 fF
Resistor	**Total Value**
R_1, R_2	≈3.52 kΩ
R_3, R_4	≈24.61 kΩ

3. Experimental Results

3.1. Low-Noise Amplifier (LNA)

Figure 5 shows a photograph of the laboratory setup used during the experimental tests for measurements of the gain and noise of the LNA. The 1.2 V voltage supply is obtained by a battery to reduce the external interference. V_{CM} is generated with the help of a potentiometer.

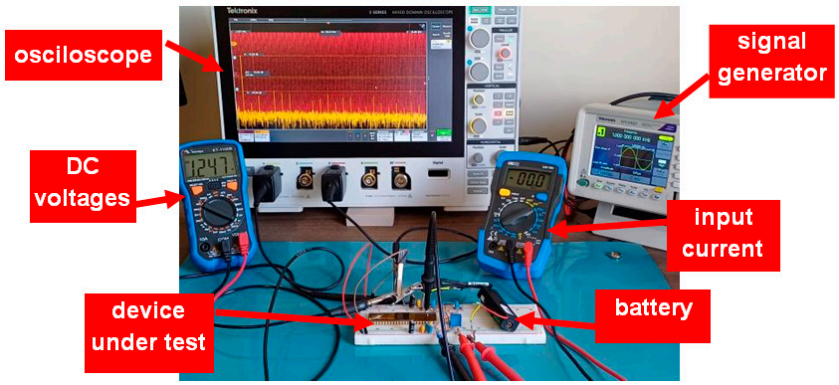


Figure 5. Photograph of the experimental setup used to obtain the gain and noise characteristics of the LNA.

Figure 6 displays the measured gain × frequency curve for several common-mode voltages (V_{CM}), different input common modes, and input signals with an amplitude of 2.2 mV_{pp}. In this set of plots, the simulation results are also shown (dotted red line) to allow for comparisons. The measurements, in general, agree well with the simulation results. The most noticeable difference between the simulated and experimental results is the positions of the cutoff frequencies. The variation in these parameters is not surprising because f_L depends on the pseudo-resistor, for which the value is difficult to estimate accurately, and f_H depends on the transistors' (M_1 and M_2's) transconductance parameter (g_m), which varies considerably in a process.

Table 3 lists the measured common-mode voltage ($V_{CM,out}$) at the output of the LNA, the maximum gain (G_{max}), and the cutoff frequencies in terms of the common-mode voltage (V_{CM}). The disparity between $V_{CM,out}$ and V_{CM} arose because of the high-value pseudo-resistors and the gate leakage currents of M_1 and M_2.

Table 3. Measured common-mode output voltage ($V_{CM,out}$), maximum gain (G_{max}), f_L, and f_H of the LNA for different V_{CM}s values.

V_{in} (mV_{pp})	V_{CM} (V)	$V_{CM,out}$ (V)	G_{max} (dB)	f_L (Hz)	f_H (kHz)
2	0.5	0.506	41.1	6.1	13
	0.6	0.63	41.2	1.5	11.5
	0.7	1.08	40.2	1.3	8

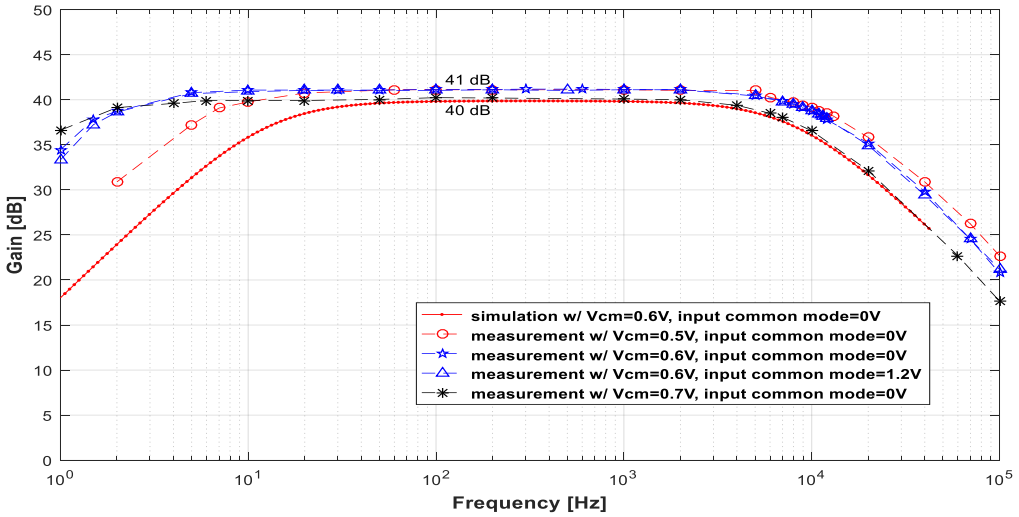


Figure 6. Plots of the measured gain × frequency curves for input signals with an amplitude of 2 mV_{pp} and several values of V_{CM} and input common modes. These plots are compared with the simulations (dotted line in red).

Notice that an elevation in the common-mode voltage (V_{CM}), as depicted in Figure 6 and Table 3, leads to a decrease in both frequencies f_L and f_H. On the other hand, variations in V_{CM} within the range of [0.5, 0.6] V did not yield significantly different gain curves. Additionally, variations in the input common mode did not alter the LNA operation. This demonstrates the robustness of the LNA concerning the input common mode, resulting in a low potential for the linear distortion of the signals during amplification.

The biasing voltage applied in the tests was V_{BIAS} = 0.75 V, obtained using a bias resistance of R_{BIAS} = 3.3 GΩ connected between the V_{BIAS} node and the ground. This resulted in a total current of I_{total} = 4.9 µA and a power consumption of 5.9 µW.

Figure 7 presents the measurement and simulation results of the input-referenced noise. The agreement between measurements and simulations is quite good for frequencies above 12 Hz, which is the low cutoff frequency found in the simulations. Below this frequency, the measured noise continues to increase because the cutoff frequency of the implemented LNA is at 1.5 Hz. The measured IRNs are 6.48 μV_{RMS} from 1.5 Hz to 200 kHz, 3.45 μV_{RMS} from 200 Hz to 11.5 kHz, and 7.36 μV_{RMS} from 1.5 Hz to 11.5 kHz.

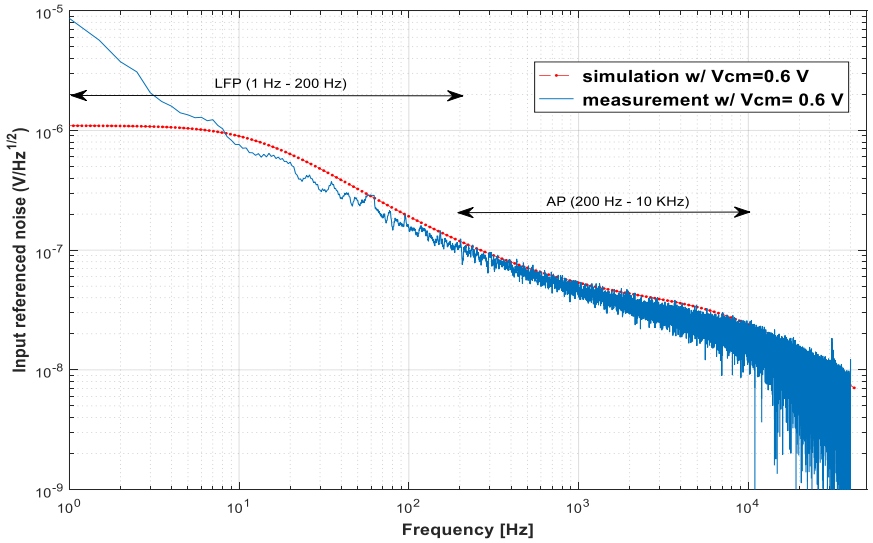


Figure 7. Plots of the measured input-referenced noise × frequency for input signals with an amplitude of 2 mV_{pp} (blue). These plots are compared with the simulations (dotted line in red).

In the LNA, the total harmonic distortion (THD) is less than −46 dB for input signals as high as 6.1 mV_{pp} or less than −51 dB for input signals as high as 4.4 mV_{pp}. The THD was calculated with the first nine harmonics.

This LNA was also tested with a saline solution to emulate an ex vivo situation and evaluate its performance in real in vivo applications. Figure 8 presents the measured gains for signals injected into the saline solution. The amplitudes of the injected signals were adjusted to obtain approximately 5 mV_{pp} at the LNA input. The voltage value of the generator output ranged between 6 mV_{pp} and 20 mV_{pp}, depending on the frequency.

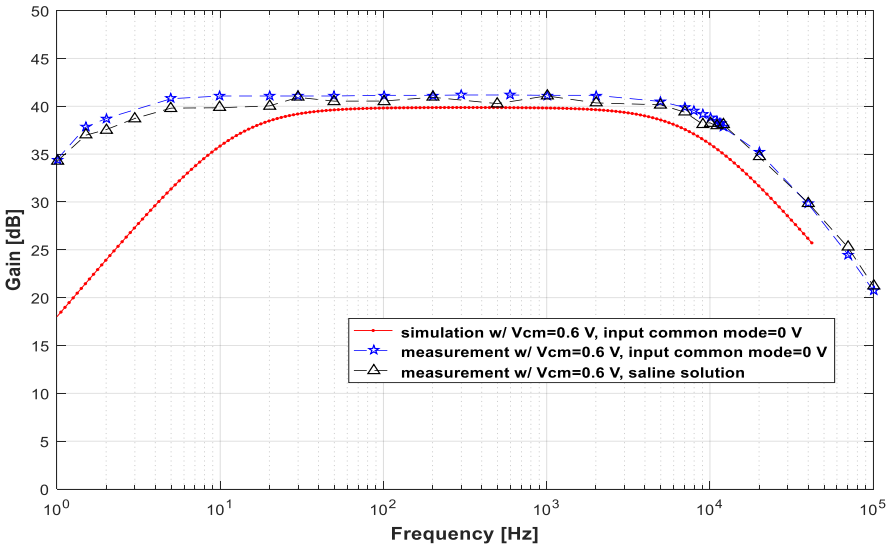


Figure 8. Plot of the measured gain × frequency for signals injected into the saline solution. The signals injected into the solution were adjusted to obtain approximately 5 mV_{pp} at the LNA input.

As seen in Figure 8, the gain did not show any appreciable reduction in the frequency range between 1 Hz and 100 kHz. In fact, it is possible to observe that the gain remained high, with its maximum value of 41.1 dB at 100 Hz.

3.2. Neurostimulator Circuit

The tests of this electronic block can be divided into static and dynamic tests. In static tests, the signals applied to the circuit do not change over time. On the contrary, in dynamic tests, the different signals vary over time. The experimental setups used for both types of tests are essentially the same, except for how the test signals were generated. The voltage (V_{BIAS}) was set at 315 mV.

Figure 9a illustrates the schematic of the experimental setup for the static characterization of the neurostimulator circuit. This setup comprises a voltage follower, implemented with the operational amplifier (TL084), to generate the common-mode voltage ($V_{CM,electrode}$) applied in the reference terminal of the electrode. The implantable electrode is represented by the load resistor (R_{LOAD}).

The common-mode voltage ($V_{CM,electrode}$) at the reference electrode was manually set between 0 V and 1.2 V in coarse steps of 0.3 V. Moreover, two breakout boards based on the MCP4725 digital-to-analog converter (DAC) with an I^2C interface were used to make fine-tuning adjustments of the inputs (V^+ and V^-) and, thus, precise adjustments of the currents injected into the load resistor (R_{LOAD}). An Arduino board was selected to control the DACs.

Figure 9b shows a photograph of the experimental setup used in the static characterization of the current pump.

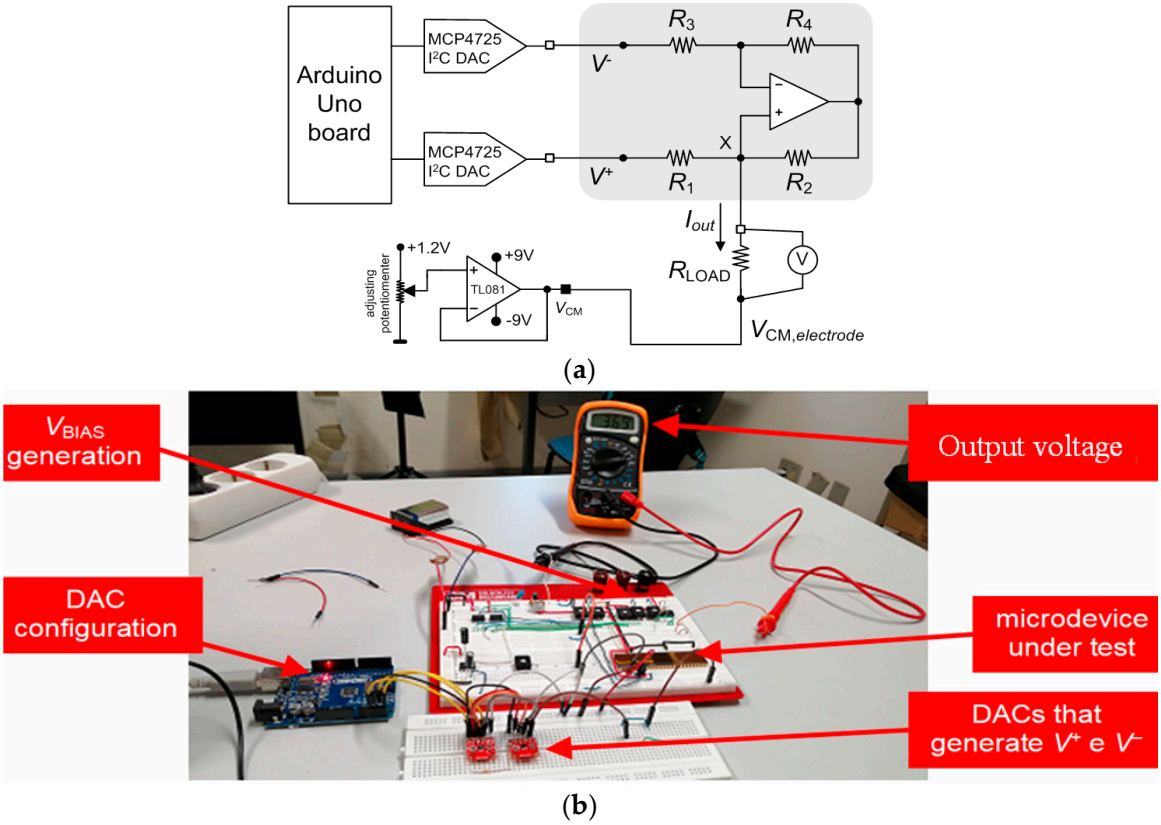


Figure 9. (**a**) Schematic of the experimental setup used in the static characterization of the neurostimulator circuit. (**b**) Photograph of the experimental setup used in the static characterization of the current pump.

Figure 10a illustrates the currents for the various combinations of the control and common-mode voltages $\{V^+, V^-, V_{CM,electrode}\}$ in "raw" form to allow for a clear and immediate visualization of the wide and quasi-symmetrical range of currents that are possible to generate with this current pump. In contrast, Figure 10b illustrates the currents parameterized in terms of the reference voltage of the electrode ($V_{CM,electrode}$) and the inverting input voltage (V^-). The output current was determined using the following expression:

$$I_{out} = \frac{V_{out} - V_{CM,electrode}}{R_{LOAD}} \quad (3)$$

A load resistance of R_{LOAD} = 986.5 Ω was used for these tests. The output voltage (V_{out}) can range from 0 V to 1.2 V; therefore, the output current (I_{out}) can either be positive or negative, simply by making the voltage of the reference electrode ($V_{CM,electrode}$) either equal to 0 V or 1.2 V, respectively. As it is possible to observe in Figure 10a,b, other intermediate currents are possible to be generated. The inversion of the current direction is mandatory in deep-brain stimulation applications.

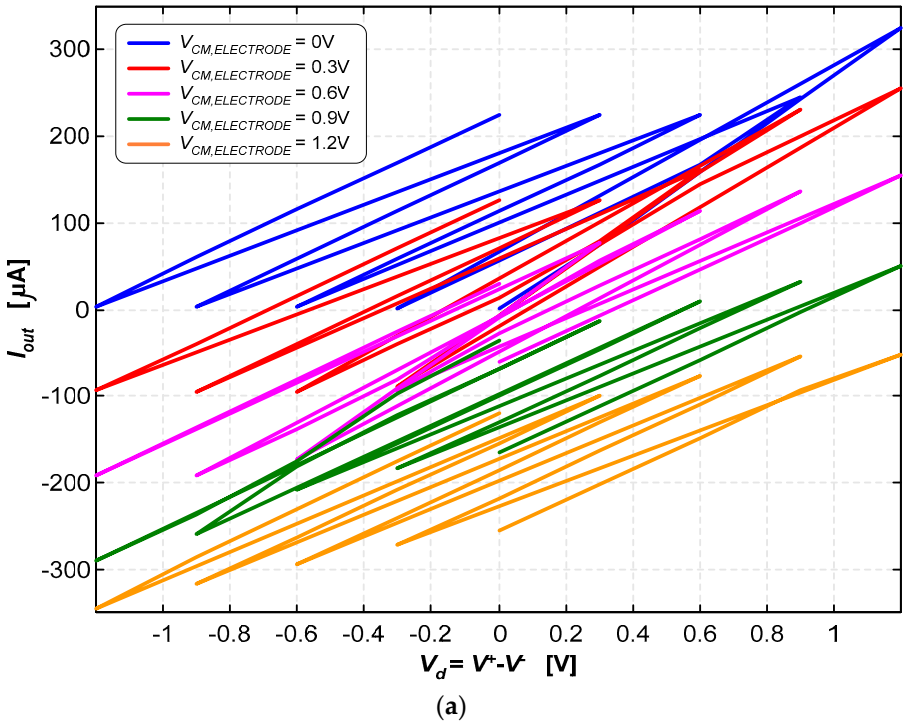
The current pump was able to generate stimulation currents ranging from −325 µA to +318 µA. The path marked with the dashed yellow lines in Figure 10b illustrates how continuous current signals can be generated within this range.

For the dynamic tests, the frequency of the signal at V^- is ten times higher than the frequency of the signal applied at V^+. The amplitudes of both signals varied between 0 V and 1.2 V. These settings result in a wave, the product of the two input waves, with a sliced sine shape. The reference voltage ($V_{CM,electrode}$) of the electrode was also manually adjusted between 0 V and 1.2 V during these tests. Figure 11 shows the experimental results of the dynamic characterization.

A set of sine waves with a common-mode voltage of 0.6 V and different amplitudes were applied in the non-inverting input (V^+), with V^- and $V_{CM,electrode}$ set at one of the voltages {0, 0.6, 1.2} V. The voltage difference (ΔV^+) in the plot is the difference between the maximum and the minimum values of the voltage (V^+). The voltage difference (ΔV^+) is equal to $2A^+$ for a non-inverting input (V^+) of $V^+ = 0.6 + A^+.\cos(2\pi ft)$. The amplitude ($\Delta V^+$) was swept from 0.2 V to 1.2 V in steps of 0.2 V. The non-inverting input (V^+) voltage variation is rail-to-rail for $A^+ = 0.6$ V. Figure 11 also shows the results for seven combinations of $\{V^-, V_{CM,electrode}\}$ in the set {0, 0.6, 1.2} V. Each combination defines the admissible range of the output current, for which plane domains are bounded above and below by two straight lines. The upper line occurs for $V^+ = 0.6 + \Delta V^+$, while the bottom line occurs for $V^+ = 0.6 - \Delta V^+$. It is possible to observe, in Figure 11, the ability to dynamically sweep the complete current limit, ranging from $I_{max} = +375$ µA to $I_{min} = -218$ µA, simply selecting the most suitable voltage combination of $\{V^+, V^-, V_{CM,electrode}\}$.

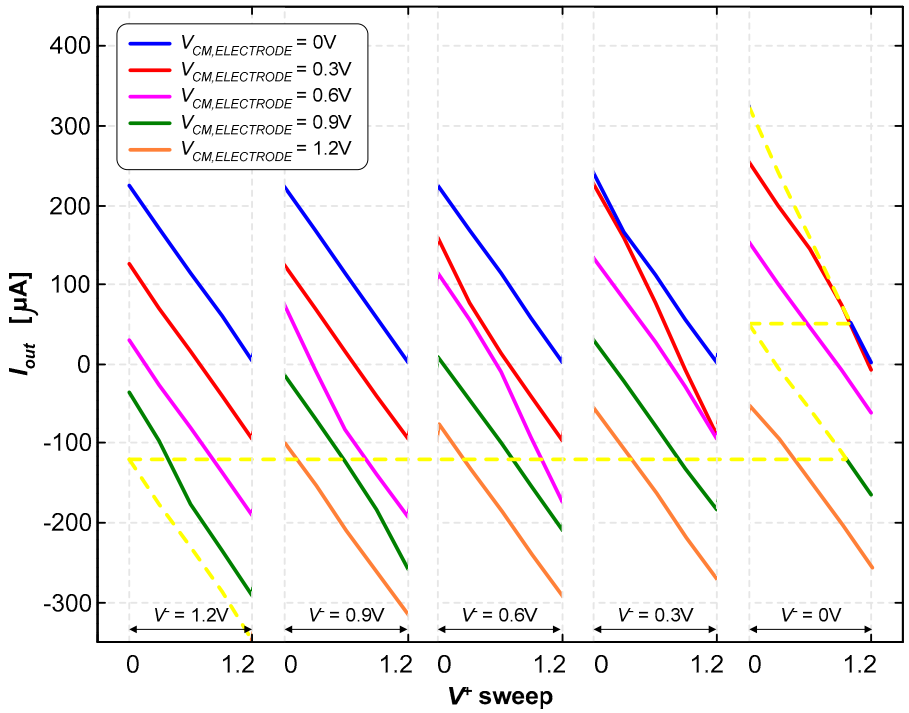
It is also possible to observe in Figure 11 that a limited set of voltage combinations of $\{V^+, V^-, V_{CM,electrode}\}$ must be avoided, under the penalty of not being able to generate very specific values of the electric current. These voltage combinations are associated with the "no-man's land" regions marked with gray shading. These "no-man's land" regions represent combinations that are not contained in the set of the seven planar domains for the different voltage combinations $\{V^+, V^-, V_{CM,electrode}\}$.

The measurements showed that these results are valid for all the voltage combinations $\{V^+, V^-, V_{CM,electrode}\}$ for a frequency of up to $f_{-3dB} = 1.5$ MHz. This frequency is the one that narrows the current range from $I_{max} - I_{min}$ to -3 dB. For example, the measurements indicated that $I_{max} = +297$ µA and $I_{min} = +248.4$ µA for $V^+ = 0.6 + 0.1\cos(2\pi ft)$ or $\Delta V^+ = 0.2$ V, with $f < f_{-3dB}/10$, $V^- = 0$ V, and $V_{CM,electrode} = 0$ V. This results in $\Delta I_{out} = I_{max} - I_{min} = +49$ µA. The measurements also showed that $\Delta I_{out} = (+49) \times (2)^{-1/2} \times (10^{-6}) = +34.6$ µA for $f = f_{-3dB} = 1.5$ MHz.



(a)

Figure 10. *Cont.*



(**b**)

Figure 10. (**a**) Stimulation currents for the various combinations of voltages, $\{V^+, V^-, V_{CM,electrode}\}$, in "raw" form to allow for a clear and immediate visualization of the wide and quasi-symmetrical range of currents. (**b**) Stimulation currents are doubly parameterized in terms of the reference voltage of the electrode (V_{CM}) and the inverting input (V^-).

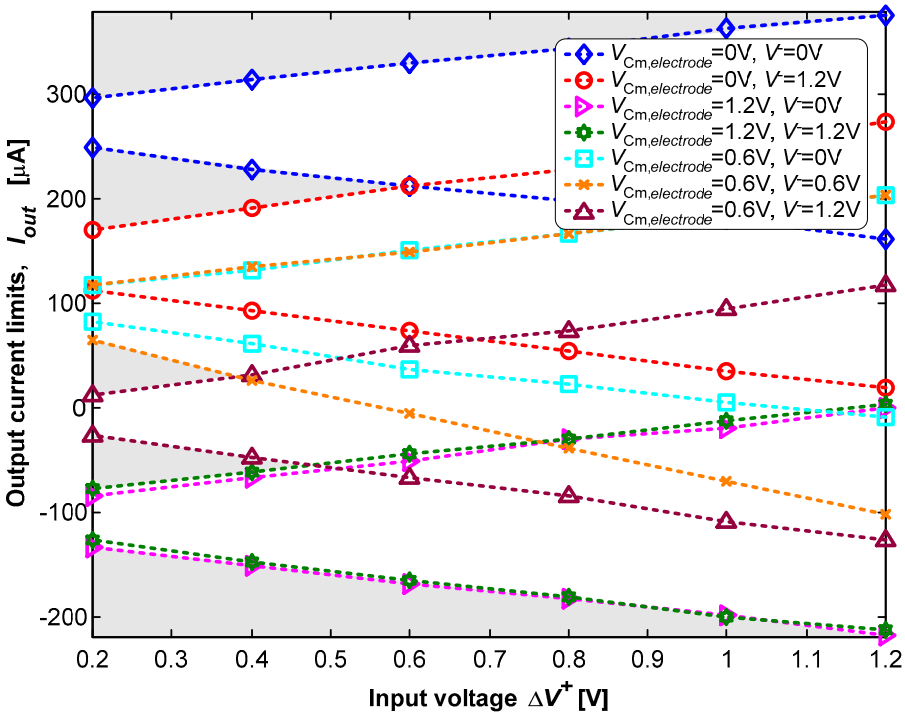


Figure 11. Dynamic characterization using sine waves with rail-to-rail amplitudes.

4. Discussion

The LNA and neurostimulator were designed and fabricated in the CMOS (65 nm) from TSMC. Table 4 compares the LNA with a few related key works found in the literature [9,10,21–23,26–31]. The figure-of-merit (FOM) was calculated to better rank and compare this work with the others with respect to the internal noise–power consumption tradeoff. The FOM applied here is the noise efficiency factor (NEF), introduced in 1987 by Steyaert et al. [32] and widely used since then. It is given as follows:

$$NEF = IRN \times \sqrt{\frac{2I_{total}}{\pi \times U_T \times (4kT) \times BW}} \quad (4)$$

where I_{total} is the total current absorbed by the amplifier stage (This current excludes the amount absorbed by the bias stage.); U_T is the thermal voltage, given by kT/q (≈26 mV at a room temperature of 300 K); k is the Boltzmann constant; T is the room temperature, expressed in Kelvin; IRN is the total RMS input-referred noise; and BW is the LNA bandwidth.

Table 4. Comparison of the proposed LNA with state-of-the-art LNAs.

Ref.	CMOS Process	Mid-Band Gain (dB)	Bandwidth (Hz)	Power Supply (V)	Power Consumption (µW)	Area (mm^2)	IRN (μV_{rms})	NEF
This work	65 nm	42	1.5–200 200–11.5 k 1.5–11.5 k	1.2	5.88	0.046	6.48 3.45 7.36	– 2.63 5.57
[21]	40 nm	25.7	200–5.0 k	1.2	2.8	N/A	5.3	4.40
[22]	65 nm	52.1	1.0–8.2 k	1.0	2.8	0.042	4.13	2.93
[23]	65 nm	46	1.0–10 k	0.5	1.5	0.0039	6.5	4.34
[26]	65 nm	30	300–10 k	0.5	2.3	0.025	5.8	4.76
[9]	90 nm	58.7	0.49–10.5 k	1.0	2.85	0.137	3.04	1.93
[27]	0.13 µm	40	0.05–0.5 k	1.0	12.1	0.072	2.2	2.90
[28]	0.18 µm	40	0.1–7.4 k	1.0	3.44	0.012	4.27	3.07
[29]	0.18 µm	40	0.05–7.5 k	1.2	4.8	0.022	3.87	3.44
[30]	0.5 µm	49.26, 60.63	0.5–300 270–12.9 k	3.3	4.12	0.0144	3.16	2.53
[31]	0.5 µm	36.1	0.3–4.7 k	1.0	0.805	0.046	3.6	1.8
[10]	0.5 µm	39.5	0.025–7.2 k	±2.5	80	0.16	2.2	4.0

It must be noted that this FOM compares the noise–power tradeoff with that of a single ideal bipolar transistor. The lower the FOM, the better will be the LNA in relation to the global noise performance.

Two important observations must be made regarding the results presented in Table 4: four of the five circuits with the lowest NEFs [10,22,27,31] use single-input CMOS-inverter-based LNAs in the first gain stage. The inverter introduced half the amount of power noise. Consequently, the NEF is reduced by $\sqrt{2}$; implementations with processes with higher minimum lengths [11,26–31] display better NEFs.

The LNA presented in this work exhibits an NEF for AP applications that is comparable to the best results found in the literature. This result is attained partly because of the sizing and optimization process performed through the application of metaheuristics.

Table 5 compares the features of the neurostimulator circuit with a few related key works found in the literature [33–39]. All the works listed in Table 5 were implemented using CMOS components. The neurostimulator presented in this paper allows for the generation of current signals with non-standard waveforms and is suitable for delayed feedback, a characteristic shared only by the neurostimulator presented in [37]. It also enables the generation of bipolar current pulses, a characteristic shared by [32,35], and provides the best current range for the lowest power supply voltage, with a ratio of

535.8 µA/V (The second-best result is presented by [36], with a ratio of 412.5 µA/V). In general, all the neurostimulators presented in this paper comply with the minimum pulse duration of 90 µs and the frequency of 130 Hz required by DBS applications.

Table 5. Comparison of the proposed neurostimulator with state-of-the-art neurostimulators.

Ref.	Current (µA)	Voltage (V)	Maximum Pulse Frequency/ Bandwidth (Hz)	Minimum Pulse Duration/ Bandwidth^{-1} (µs)	Charge Balance	Active Charge Balancing Method
This work	from −325 to +318	1.2	1.5×10^6 (BW)	25	Active	Continuous (Howland current pump)
[33]	from 20 to 2000	12	500	10	Active	Switched (H-bridge)
[34]	from −200 to +200	3.6 (bat)	185	90	Active	Switched
[35]	from 0 to 200	3.2 (bat)	130	90	Passive	Switched
[36]	from 30 to 1000	3.7 (bat)	5000	10	Active	Switched
[37]	from −375 to +250	10	5000	20	Active	Continuous (Howland current pump)
[38]	from 20 to 2000	4.8 (bat)	300	40	Active	Switched (H-bridge)
[39]	from 10 to 500	3.1 (bat)	200	60	Passive	Switched

To conclude, Figure 12 depicts a photograph of the fabricated CMOS integrated circuit housing both the LNA and the neurostimulator, which occupies 1.8 mm × 1.8 mm of area. The figure emphasizes the two circuits presented in this paper.

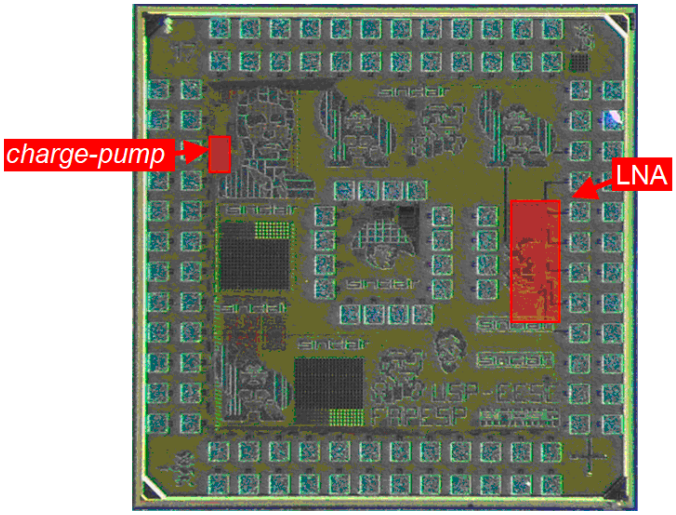


Figure 12. Photograph of the fabricated CMOS microdevice (1.8 mm × 1.8 mm), with emphasis on the LNA and the current pump presented in the paper.

5. Conclusions

Deep-brain stimulation (DBS) stands as a remarkably effective medical treatment, significantly enhancing the quality of life for patients. Closed-loop deep-brain stimulation (CLDBS) further elevates this treatment by automatically adapting the stimulation parameters. This paper presents the implementation of two crucial circuits for CLDBS, the low-noise amplifier (LNA) and the neurostimulator, both fabricated using a 65 nm CMOS process. The implemented LNA presents an NEF for AP signals, ranging from 20 Hz to 11.5 kHz, compatible with the performance of the best circuits in the literature (NEF = 2.63). Moreover, its total noise from 1.5 Hz to 11.5 kHz is 7.36 μV_{rms}, which is below the levels of

thermal and biological noises. This feature made it suitable for applications involving both LFP and AP signals. The implemented neurostimulator provides biphasic current pulses with non-standard waveforms and is suitable for delayed feedback.

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Conflicts of Interest: The authors declare no conflicts of interest.

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