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Optics Communications

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Silicon modulator design using a system-oriented methodology for high-speed data center interconnect PAM-4 applications[‡]



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ARTICLE INFO ABSTRACT Keywords: Silicon (Si) modulator and a design methodology using a system-oriented numerical approach are proposed. Silicon photonics A Silicon (Si) modulator and a design methodology using a system-oriented numerical approach are proposed. The main contributions of this work are to provide a Silicon modulator as an alternative solution for intra-data center interconnect (DCI) applications and a single figure-of-merit (FOM) for the modulator design, which takes as input the main device parameters (modulation efficiency (V_x × L), optical loss, and electro-optical takes and the system-oriented design.

1. Introduction

With the incessant growing demand for services with high bandwidth and high speed, such as cloud storage, social media, videoon-demand (VoD) and internet, the traffic load in data centers is on high alert. A report by Cisco [1] shows that the amount of annual global data center internet protocol (IP) traffic in 2021 is estimated to be 20.6ZB, 1.2x greater than the prediction for 2020. Short-reach fiber-optic communication technologies are a promising solution to fulfill the growing demand for data center traffic. Among these technologies, power-efficient and high-speed optical modulators are the key components for optical communication links. Conventionally, for short-reach links (intra-DCI up to 10km), these modulators are designed to operate with on–off keying (OOK) format. The 40 Gbit s⁻¹ and 100 Gbit s⁻¹ IEEE Ethernet standard using OOK modulation has been widely used. However, to increase the transmission capacity, the 4-level pulse amplitude modulation (PAM-4) format was recently selected by the 400 Gbit s⁻¹ IEEE Ethernet standard [2]. In this scenario, a driving voltage $\leq 3.5 \text{ V}$ [3], 1.31 µm wavelength, and optical loss $\leq 5 \text{ dB}$ are desirable, since the driver [4] and optical amplifier are generally not used. In terms of bandwidth, above 36 GHz [5] is desirable for 56 GBd

PAM-4 applications. Therefore, the improvement of optical modulators is being treated as the main challenge of this stage, since in intra-DCI power consumption is critical due to the large number of connections over short distances, and high bandwidth must be provided.

bandwidth (f_{3dB}) and provides a global optical system optimization. By using a numerical approach, the modulator physical parameters are analyzed according to system performance metrics such as the required receiver sensitivity to reach a target bit error rate (BER), and the required transmitter launch power. A capacitive Silicon device and a 4-level pulse amplitude modulation (PAM-4) system simulator is presented. The results show an efficient modulator ($V_{\pi} = 3.5$ V) with high bandwidth ($f_{3dB} > 38$ GHz), which is promising

for data centers solutions, where power consumption is critical and high-speed is required.

Several photonic modulators configurations have been proposed and improved to fulfill this need. Among different platforms for modulator design, the most popular types are based on Lithium Niobate (LiNbO₃) modulators [6,7], Indium Phosphide (InP) modulators [8,9], Silicon (Si) pn junction modulators [10,11] and capacitive modulators [12,13]. However, it is still challenging to propose a modulator for low power and high bandwidth operation. Silicon-photonics-based modulators have the advantage of compatibility with complementary metal-oxide-semiconductor (CMOS) process, which can enable mass production and integration with electronics. Unlike the popular Si pn junction modulators that use a traveling-wave (TW) transmission line, capacitive devices have better modulation efficiency and can be designed in shorter lengths (units of millimeter), resulting in a simpler driving circuit, better known as lumped-type modulators. Thus, the advantage of having a short modulator is the simplicity of the radiofrequency (RF) design (lumped element), as it does not require a

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https://doi.org/10.1016/j.optcom.2021.126977

Received 12 January 2021; Received in revised form 20 March 2021; Accepted 22 March 2021 Available online 29 March 2021 0030-4018/© 2021 Elsevier B.V. All rights reserved.

^{*} This work was supported in part by the Coordenação de Aperfeiçoamento de Pessoal de Nível Superior (Brazil, CAPES - Finance Code 001) and in part by the Fundação de Amparo à Pesquisa do Estado de São Paulo (Brazil, FAPESP - Finance Code 2016/20615-8).

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Fig. 1. Cross-section view of the capacitive Si modulator with V-shaped SiO₂ gate.

traveling-wave project. In addition, lumped-type modulators are more power efficient than TW-type devices. For these reasons, our paper proposes a capacitive Si modulator meeting all requirements for intra-DCI applications, i.e. PAM-4 at 1.31 µm wavelength, $V_{\pi} \leq 3.5$ V (without driver amplifier for low power consumption), loss ≤ 5 dB, and bandwidth > 36 GHz.

Typically, the modulator performance is assessed in terms of modulation efficiency ($V_{\pi} \times L$), optical loss, and electro-optical bandwidth (f_{3dR}) . Another challenge in photonic modulators is to find a figureof-merit (FOM) that relates $V_{\pi} \times L$, loss, and f_{3dB} to provide the best trade-off. To perform this, a few authors [14-16] have proposed a single modulator FOM using analytical methods to characterize the overall performance of a Silicon modulator (typically TW) for a specific modulation format (e.g. OOK or PAM-4), which is generally denoted as optical modulation amplitude (OMA). However, unlike the traditional analytical methodologies found in the literature, through numerical methods, this study proposes a system-oriented design methodology using PAM-4 modulation format applied to a capacitive modulator. Even though the numerical method may add some computational effort compared to the analytical one, in the proposed approach this additional workload is marginal. The analytical method is fully analytical so its computational complexity is almost negligible. For the proposed method, each calculation can take up to tens of seconds, so in order to evaluate a set of thousands of parameters, it could take as long as tens of hours, which is still reasonable for such a device optimization. The proposed work relates the main figures-of-merit ($V_{\pi} \times L$, loss, and f_{3dB}) through a complete system level approach, i.e. signal transmission, optical communication link and signal reception up to BER calculation. Then, the system optimizes the device's geometry based on the modulator performance parameters, i.e. the transmitter launch power required for a target BER. Compared to the analytical approach, the system simulator adds flexibility to the design, in which many different scenarios can be analyzed.

The paper is organized in four parts. Section 2 addresses the modulator structure as well as its main FOMs that will be applied in the system. Section 3 shows how the simulation hierarchy was organized using the building block diagram. After presenting the simulation parameters, in Section 4, the main results in a diversified scenario of the modulator configuration are presented and discussed. Finally, Section 5 presents a brief conclusion.

2. Capacitive modulator with v-shaped oxide gate

Taking into account our previous study [17], Fig. 1 shows the V-shaped SiO₂ gate Si modulator. However, unlike the previous approach, the modulator is designed with $\lambda = 1.31 \,\mu\text{m}$, targeting intra-DCI 400 Gbit s⁻¹ PAM-4 applications.

In Fig. 1, doping concentrations are symmetrical between the *p*-type and the *n*-type. To decrease the electrical access resistance to the waveguide, n_{++}/p_{++} was set to 1×10^{20} cm⁻³ and n_{+}/p_{+} was set to 1×10^{19} cm⁻³. The other parameters were set to $w_{wg} = 400$ nm, $t_{Si} = 220$ nm, $t_{poly-Si} = 160$ nm, min $t_{gate} = 5$ nm, $w_1 = 300$ nm, $w_2 = 200$ nm, and $t_{slab} = 70$ nm, which are in accordance with the study presented in [17] to optimize the modulator performance and a few trade-offs.

2.1. Analysis of vpil! and optical loss

The refractive index (Δn) and absorption ($\Delta \alpha$) change as function of the charge concentration is calculated using Soref's equations for 1.31 µm wavelength, according to (1) and (2) [18],

$$\Delta n(x, y) = -6.2 \times 10^{-22} N_e(x, y) - 6 \times 10^{-18} N_h^{0.8}(x, y)$$
⁽¹⁾

$$\Delta \alpha (x, y) = 6 \times 10^{-18} N_e(x, y) + 4 \times 10^{-18} N_h(x, y)$$
⁽²⁾

where N_e and N_h are the electrons and holes concentrations, respectively.

In the case of modulators that have a Silicon waveguide, when subjected to a voltage, the figure-of-merit $V_{\pi} \times L$ varies non-linearly due to the non-linear change of the Si refractive index. In this way, the modulation efficiency, given in V m, can be calculated according to (4) [19],

$$n_{eff} = \frac{\iint_{\infty} \left[n_{Si} + \Delta n(x, y) \right] |E(x, y)|^2 \, ds}{\iint_{\infty} |E(x, y)|^2 \, ds} \tag{3}$$

$$V_{\pi} \times L = \frac{\lambda}{2} \frac{dV_{bias}}{dn_{eff}} \tag{4}$$

where n_{eff} is the effective index, n_{Si} is the Si refractive index, E(x, y) is the fundamental mode electric field distribution, and λ is the wavelength.

Optical losses occur mainly due to phase-shifter doping. In this case, this FOM, given in $dB m^{-1}$, is found according to (5),

$$Loss = \frac{40\pi\Im\left\{n_{eff}\right\}}{\lambda}\log_{10}e\tag{5}$$

where imaginary part of the effective index is the imaginary part of the effective index.

The phase shift (Ψ), given in rad m⁻¹, is calculated according to (7) [20],

$$\Delta n_{eff} = \Re \left\{ n_{eff} \left(V_{bias} \right) - n_{eff} \left(0 \right) \right\}$$
(6)

$$\Psi = \frac{2\pi}{\lambda} \Delta n_{eff} \tag{7}$$



Fig. 2. (a) Modulation efficiency in several design scenarios of *d* and max t_{gate} , for $V_{bias} = 0$ V and 5×10^{17} cm⁻³ p/n doping. (b) $V_{\pi} \times L$ and its corresponding loss as function of V_{bias} , for max $t_{gate} = 150$ nm and 5×10^{17} cm⁻³ p/n doping. (c) Loss as function of doping concentration, for $V_{bias} = -5$ V and max $t_{gate} = 150$ nm. (d) Phase shift as function of V_{bias} , for max $t_{gate} = 150$ nm and 5×10^{18} cm⁻³ p/n doping.

which takes into account the subtraction between the final and initial points of real n_{eff} according to the applied V_{bias} .

The results of $V_{\pi} \times L$, Loss, and Ψ were extracted by LUMERICAL software. Fig. 2 shows the device behavior in several scenarios.

Observing Fig. 2(a), it is concluded that the modulation efficiency can be optimized by means of *d* and max t_{gate} . Basically, higher *d* with lower max t_{gate} improves modulation efficiency (lower $V_{\pi} \times L$). In Figs. 2(b)–2(d), parameter max t_{gate} was set to 150 nm in order to increase bandwidth (to be explained in Section 2.2). To further improve $V_{\pi} \times L$, reverse bias voltage must be increased, as shown in Fig. 2(b). However, optical loss also increases.

In Fig. 2(c), it is observed that, for a high voltage ($V_{bias} = -5$ V), when increasing doping concentration, the optical loss increases exponentially. On the other hand, in the next section it will be seen that this scenario improves the bandwidth. In addition, Fig. 2(c) shows that, even in a scenario of high doping ($5 \times 10^{18} \text{ cm}^{-3}$), the optical loss is acceptable ($\leq 15.33 \text{ dB mm}^{-1}$) for waveguide length (L_{wg}) < $326 \,\mu\text{m}$. Finally, Fig. 2(d) shows higher phase shift for higher voltages. Therefore, from these analyzes, V_{bias} is set to -5 V to achieve higher phase shift (or lower $V_{\pi} \times L$).

2.2. Bandwidth analysis

Taking into account the slabs resistivity (ρ) and phase-shifter SiO₂ gate capacitance (C_{gate}) (extracted from numerical software), electrooptical bandwidth was obtained through an analytical model implemented in MATLAB according to [17], as shown in Fig. 3.

In Fig. 3(a), the higher the doping concentration, the lower the resistivity. This scenario improves bandwidth (compare Figs. 3(c), 3(e), and 3(f)), but increases optical loss (see Fig. 2(c)). Fig. 3(b) shows the capacitance behavior as a function of *d* and *max* t_{gate} . For high bandwidth, the phase-shifter must have low capacitance. However,

Fig. 3(b) shows that this behavior is contrary to the $V_{\pi} \times L$ presented in Section 2.1 (see Fig. 2(a)). Therefore, higher max t_{gate} should be used for higher bandwidth. This scenario does not significantly affect $V_{\pi} \times L$ if higher d is used at high voltages (see Fig. 2(b)). In addition, comparing Figs. 3(c) and 3(d), it is concluded that a shorter device (low L_{wg}) improves bandwidth (due to lower capacitance, since C_{gate} is given in F m⁻¹). On the other hand, this condition results in higher V_{π} , since $V_{\pi} \times L$ is given in V m.

In principle, perform a graphical analysis to choose the ideal tradeoff between modulation efficiency, optical loss, and bandwidth is not an efficient way to express the best performance that the modulator can achieve, since a system-level analysis of the device would not be taken into account. Therefore, designing a Mach–Zehnder modulator (MZM) in this scenario is not a simple task. For this, a case study of the waveguide doping (*n*-type & *p*-type) and length (L_{wg}) is considered, which, along with *d* and max t_{gale} parameters, are used to optimize the modulator parameters by minimizing the CW laser launch power required at the transmitter for a given system.

3. System simulator structure

An optical system simulator was set-up in Python language to evaluate the system performance according to different modulator parameters. The building block diagram of the system is shown in Fig. 4.

The simulator is focused on PAM-4 systems at $1.31 \,\mu$ m, but it can be adapted to any modulation format with simple modifications. The simulator is implemented in the time domain, where the entire signal is processed at each block. Filtering is done at frequency domain by taking the Fourier transform of the time-domain signal (and back after



Fig. 3. (a) Slabs resistivity as a function of doping concentration. (b) SiO_2 gate capacitance for 5×10^{17} cm⁻³ p/n doping. (c) Bandwidth for 5×10^{17} cm⁻³ p/n doping and $L_{wg} = 200 \,\mu$ m. (d) Bandwidth for 5×10^{17} cm⁻³ p/n doping and $L_{wg} = 500 \,\mu$ m. (e) Bandwidth for 1×10^{18} cm⁻³ p/n doping and $L_{wg} = 200 \,\mu$ m. (f) Bandwidth for 5×10^{17} cm⁻³ p/n doping and $L_{wg} = 200 \,\mu$ m.

filtering). Eq. (8) shows the transfer function of the Gaussian low-pass filter (LP_G) [21],

$$LP_G = e^{-\ln\left(\sqrt{2}\right) \left(\frac{f}{\Delta f_G}\right)^{2\eta}} \tag{8}$$

where f is the frequency, Δf_G is the filter bandwidth, and η is the filter order.

The CW phase noise is modeled using a random variable in the phase term with normal distribution, with the variance being related to the laser linewidth. The Mach–Zehnder modulator model takes as input the modulator $V_{\pi} \times L$, optical loss, f_{3dB} , and bias operating point (OP). Eq. (9) shows the MZM's output electric field (E_{out}) as a function of its input electric field (E_{in}),

$$E_{out} = \frac{E_{in}}{2} \left(e^{j\Psi_A L_{wg}} + e^{j\Psi_B L_{wg}} \right)$$
⁽⁹⁾

where L_{wg} is the phase-shifter length and Ψ_A and Ψ_B are the phase shift for each MZM arm, which are calculated according to (7). The MZM is implemented in push–pull configuration.

At the receiver side, shot noise and thermal noise were considered in the photodiode. They are the two fundamental noise mechanisms responsible for current fluctuations in all optical receivers, even when the incident optical power is constant [22]. Shot noise is a quantum noise effect, related to the discreteness of photons and electrons [23]. The shot noise variance is obtained as [22]:

$$\sigma_s^2 = 2e\left(I_p + I_d\right)\Delta f \tag{10}$$

where *e* is the electronic charge, I_p is the average photodiode current, I_d is the dark current, and Δf is the effective noise bandwidth of the receiver.



Fig. 4. Building block diagram: pseudo-random binary sequence (PRBS) generator, digital-to-analog converter (DAC), analog-to-digital converter (ADC), automatic gain controller (AGC), transimpedance amplifier (TIA), variable optical attenuator (VOA), photodiode (PD), continuous-wave (CW) laser, and Mach–Zehnder modulator (MZM).



Fig. 5. Example for calculating sensitivity in different modulator length scenarios, for 5×10^{17} cm⁻³ p/n doping, d = 100 nm, and max $t_{eac} = 150$ nm.

At the front end of an optical receiver, there is a load resistor (R_L) that adds fluctuations to the current generated by the photodiode due to the random thermal motion of electrons. This additional noise component is known as thermal noise. The thermal noise variance is calculated as [22]:

$$\sigma_T^2 = \frac{4k_B T}{R_L} F_n \Delta f \tag{11}$$

where K_B is the Boltzmann constant, T is the absolute temperature, and F_n represents the factor by which thermal noise is enhanced by various resistors used in amplifiers.

Finally, the total current noise variance can be obtained by adding the contributions of shot noise and thermal noise according to (12) [22].

$$\sigma^2 = \sigma_s^2 + \sigma_T^2 \tag{12}$$

Transimpedance amplifiers (TIAs) are used at the front end of optical receivers. In optical communications, the TIA is a fast and sensitive current measuring device. Normally, a weak current signal originating from a photodetector is amplified and converted to a voltage signal [24]. Finally, at TIA, Gaussian noise was used.

Table 1 Simulation parameters.							
Block	Parameter	Value	Unit				
Laser	Linewidth	1	[MHz]				
Driver	Bandwidth	50	[GHz]				
DAC	ENOB	6	[bit]				
	Bandwidth	50	[GHz]				
TIA	Gain	5	[kΩ]				
	NEP	10	[pA/√Hz]				
	Bandwidth	43	[GHz]				
ADC	ENOB	6	[bit]				
	Bandwidth	50	[GHz]				
	Input V _{pp}	1	[V]				
Coupling loss		0.5	[dB]				
PD Responsitivity		1	[A W ⁻¹]				
Dark current		80	[nA]				
Bandwidth		50	[GHz]				

Table 2

Parameters and FOMs fitted to offer the best trade-off.

<i>p/n</i> doping [cm ⁻³]	d [nm]	max t _{gate} [nm]	L _{wg} [µm]	Sensitivity [dBm]	Min P _{CW} [dBm]
5×10^{17}	100	150	200	-15.84	2.34
1×10^{18}	100	150	200	-16.04	2.38
5×10^{18}	100	150	200	-15.32	4.76

4. System-oriented modulator optimization results

Based on the building block diagram presented in Fig. 4, Table 1 shows the main simulation parameters. Throughout the analysis, the system operated with non-return-to-zero (NRZ) pulse format, 56 GBd symbol rate, and 2×10^{18} transmitted symbols. The signal is upsampled by a factor of 2 and 16 in the digital and analog domains, respectively.

Considering 10 dB passive loss (PL), 0.4 dB km^{-1} fiber loss (FL), and 10 km fiber length (L_{fiber}), the required CW launch power (P_{CW}) can be calculated according to (14):

$$OPL = -10 \log_{10} \left(\frac{V_{bias}}{V_{\pi}} \right)$$
(13)

 $P_{CW} = \text{Sensitivity} + \text{PL} + \text{OPL} + \text{MZM Loss} + \text{FL} \times L_{fiber}$ (14)

where (13) expresses the MZM operating point loss (OPL).

As a first step, the system sensitivity is calculated. For this, a sweep in the BER versus the received optical power (ROP) is performed. Then,



Fig. 6. Sensitivity and CW launch power. (a) & (b) 5×10^{17} cm⁻³ p/n doping and $L_{wg} = 200 \,\mu\text{m}$. (c) & (d) 1×10^{18} cm⁻³ p/n doping and $L_{wg} = 200 \,\mu\text{m}$. (e) & (f) 5×10^{18} cm⁻³ p/n doping and $L_{wg} = 200 \,\mu\text{m}$.

the sensitivity is the ROP value corresponding to the target BER, as shown in (15).

$$Sensitivity = ROP\Big|_{Target BER}$$
(15)

Fig. 5 shows typical curves of BER as function of the received optical power for different modulator design scenarios with 5×10^{17} cm⁻³ p/n doping. The sensitivity is the received optical power required to achieve the target BER (red dashed line).

During the simulation, the parameters were swept in the following range: d = 5 nm to 100 nm, max $t_{gate} = 10 \text{ nm}$ to 150 nm, and $L_{wg} = 100 \mu\text{m}$ to $1000 \mu\text{m}$. The doping concentration was evaluated at three levels, $5 \times 10^{17} \text{ cm}^{-3}$, $1 \times 10^{18} \text{ cm}^{-3}$, and $5 \times 10^{18} \text{ cm}^{-3}$. For 56 GBd symbol rate, the cutoff frequency was set to 36 GHz to achieve the target BER (3.8×10^{-3}). This means that for every device geometry with bandwidth < 36 GHz will be disregarded, because the system would not achieve the

target BER even for high received powers. Finally, the system model was set to operate at quadrature bias point with peak-to-peak voltage $V_{pp} = 3.5$ V. Taking into account all sweep options, Fig. 6 shows only those containing the lowest P_{CW} for each doping considered.

Based on Fig. 1, when the *d* reach increases, the thick SiO₂ gate area is decreased, resulting in higher capacitances (low bandwidth). For this reason, the blank areas in Fig. 6 correspond to ignored values, since $f_{3dB} < 36$ GHz in these regions. The analysis for max t_{gate} is done in a similar way. Now, analyzing the device p/n doping, when the concentration increases (see Figs. 6(a), 6(b) to Figs. 6(e), 6(f)), the modulator provides higher bandwidth (larger non-white area), however, it is observed that the CW launch power is affected. The improvement in bandwidth is related to the lower electric access resistance. On the other hand, the increase of CW launch power is related to the increase in optical loss.



Fig. 7. Eye diagrams based on the adjustment parameters in Table 2. (a) 5×10^{17} cm⁻³ p/n doping. (b) 1×10^{18} cm⁻³ p/n doping. (c) 5×10^{18} cm⁻³ p/n doping.

Since the system has already chosen the best L_{wg} among all possibilities in Fig. 6, the next step is to minimize the CW launch power by adjusting *d* and max t_{gate} for each doping concentration considered. Table 2 shows several figures-of-merit (FOMs) optimized to obtain the lowest P_{CW} together to the sensitivity that the modulator can offer.

Note that, in Table 2, among the three doping considered, the one that offers the lowest CW launch power is the concentration of 5×10^{17} cm⁻³, corresponding to 2.34 dBm. In this case, Table 2 also shows the adjustment parameters (*d*, max t_{gate} , and L_{wg}) to reach this FOM, as well as the corresponding sensitivity.

Even though it is the best configuration for this specific structure, the modulator, through the analyzed parameters, can be adapted for any other application, depending on the designer's goals. Fig. 7 shows the eye diagrams for each configuration defined in Table 2. Note that, clear and open eyes are demonstrated, indicating high quality of the transmitted signal.

5. Conclusions

In this paper, a Si modulation device and a methodology to adjust the physical and geometrical parameters of photonic modulators through a system-oriented design were proposed. A capacitive modulator with three doping concentration levels in the waveguide was analyzed. Figures-of-merit such as modulation efficiency, optical loss and bandwidth were applied as inputs to the simulator and evaluated at the system performance level, i.e. from the transmission to the reception of a PAM-4 signal through an optical link. Then, the best modulator adjustment parameters were selected to solve the trade-off problem between the FOMs.

According to the results, the modulator proved to be more efficient in a lower doping concentration among the three addressed. In this case, for a concentration of 5×10^{17} cm⁻³, the device reached CW launch power equal to 2.34 dBm and sensitivity of -15.84 dBm, with device parameters d = 100 nm, max $t_{gate} = 150$ nm, and $L_{wg} = 200 \,\mu\text{m}$. In this scenario, the modulator will operate with $V_{\pi} = 3.5$ V, Loss ≈ 1.2 dB, and $f_{3dB} > 38$ GHz, which is in line with intra-DCI requirements. For comparison, a state-of-the-art capacitive modulator has been demonstrated in [25] with $L_{wg} = 200 \,\mu\text{m}$, $V_{\pi} \times L = 1.8$ V cm, Loss < 1 dB, and electro-optical bandwidth > 35 GHz. Note that, the V-shaped oxide gate modulator is ~ 25x more efficient in terms of modulation efficiency, with similar optical loss and bandwidth. Therefore, the V-shaped SiO₂ gate modulator is promising for future data center applications.

Finally, although only one type of modulator was used to evaluate the system, the content covered in this study will be useful as a tool for photonic device designers, since this methodology can be applied to any type of optical modulator with its own geometrical and physical characteristics operating in any modulation format.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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