Capacitive Silicon Modulator Design with V-shaped SiO_2 Gate Waveguide to Optimize $V_\pi \times L$ and Bandwidth Trade-off

Diego M. Dourado, Giovanni B. de Farias, Yesica R. R. Bustamante, *Member, IEEE*, Mônica de L. Rocha, *Member, IEEE*, and J. P. Carmo

***Abstract*—This work presents a capacitive modulator design and modeling of a new waveguide architecture using silicon and poly-si technologies. We use a methodology involving the entire lumped-type modulator design process, from the optical design to the small-signal RF analysis. By means of geometric and physical parameters adjustments, the trade-offs among several figures of merit are analyzed in this paper. Due to the waveguide configuration, it is shown that the modulator can improve the trade-off between V_π and bandwidth compared to the state-of-the-art for this kind of device. For instance, the best combinations are $V_\pi \simeq$ 1 V @ 20.4 GHz and V_π = 5.7 V @ ∼31 GHz, with equivalent optical losses of 3 dB and 1.1 dB, respectively.**

***Index Terms*—capacitive modulator, figure of merit, V-shaped oxide gate modulators, lumped-type modulator, mach-zehnder, optical devices, silicon photonics, trade-off analysis.**

I. Introduction

SILICON photonics (SiPh) has evolved to competitive levels of performance and scaling as a technology platform for complex photonic integrated circuits (PIC). Leveraging the development of new devices in several application fields, including telecommunications and data communications, Europe is in a leading position in generic integration platforms [1]. With the European Commission's effort to boost the industrial competitiveness of SiPh technology, the value of PIC markets is expected to increase to multi-billion dollar levels in the coming years. Chip-level photonic interconnect is expected to generate almost $1B by 2020 [1]. This scenario is related to the exponential increase in data consumption, since new technologies must be developed to deliver optical transceivers with lower power consumption and higher capacity. For datacom applications, where the driver and optical amplifier are generally not used, the driving voltage should be <2 V and the optical loss <5 dB. On the other hand, for telecom applications, a higher driving voltage may be considered (e.g. 8 V), since a driver amplifier is generally used. In terms of bandwidth, for 56 Gbaud applications, 36 GHz for PAM-4 modulation is desirable [2], whereas for 28 Gbaud or 32 Gbaud, a bandwidth between 20 GHz and 25 GHz can be considered.

Several silicon photonic modulators configurations have been investigated to fulfill this need. The most popular type of silicon modulators are based on the carrier depletion mechanism (e.g. $V_\pi \times L \simeq$ 1.28 V.cm and $Loss \simeq$ 3.33 dB/mm [3]). To provide enough modulation efficiency (V_π = 8.5 V), these modulators need to be relatively long (in general above 1.5 mm), which requires a travelling wave design [4], [5], [6], [7].

Capacitive modulators have been investigated since the early 2000s [8]. They use the carrier accumulation mechanism, which can improve modulation efficiency ($V_\pi \times L$) by an order of magnitude compared to carrier depletion. Such devices can be designed with short lengths (<1 mm) and, even so, offer acceptable V_π, behaving as lumped-type modulators. Although treated for a long time as a promising solution for high-speed devices, optimizing the trade-off between modulation efficiency and bandwidth is still challenging. This fact is related to the oxide gate thickness. For instance, considering a capacitive modulator with thin oxide gate thickness (e.g. 5 nm [9]), the V_π can be in the order of 9 V, but with limited bandwidth (∼10 GHz). On the other hand, increasing the gate thickness to 35 nm [9], the bandwidth can be improved to about 30 GHz, sacrificing the V_π to 32.8 V. Therefore, the conventional silicon capacitive modulator [10] can not achieve feasible values of V_π and bandwidth at the same time.

For these reasons, and unlike all capacitive modulators shown in the literature, our modulator addresses a waveguide with V-shaped oxide gate thickness to optimize the trade-off problem between modulation efficiency and bandwidth. In this way, it is possible to decrease the gate capacitance to provide high bandwidth and, at the same time, to keep V_π low even if it is adjusted for short lengths. Several parameters are evaluated to fit the best design scenario and offer the lowest V_π combined with the highest bandwidth that the modulator can offer.

The modulator proposed in this work was evaluated in simulation according to two active device lengths, 250 μm and 500 μm, which were chosen in order to compare with recent state-of-the-art references. In a scenario that offers low V_π (∼1 V), the proposed device has an estimated bandwidth of 20.4 GHz. In another configuration, the bandwidth can be improved to ∼31 GHz with a V_π of 5.7 V. On the other hand, in a scenario of higher V_π (14.2 V), the modulator

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presented bandwidth of ∼39 GHz.

The paper is organized in seven parts. Section II addresses the modulator structure that will be modeled based on available SOI technologies. By means of modal analysis, in section III the waveguide design is discussed. Section IV presents an analysis of $V_\pi \times L$ and optical loss in several design scenarios. Section V performs a dynamic evaluation of the modulator by means of RF analysis and presents an optical modulation amplitude (OMA) evaluation to address system performance. Section VI performs a brief study of the fabrication feasibility for the proposed waveguide architecture. Finally, section VII presents the conclusion and a comparison between the proposed solution (a few design scenarios) and the state-of-the-art.

II. Modulator Structure

Fig. 1 shows the proposed modulator with V-shaped SiO_2 gate. Thus, keeping the central SiO_2 gate width constant to a certain reach (d), the waveguide is efficient during the refractive index change and the $V_\pi \times L$ is minimized. On the other hand, by varying the oxide gate thickness ($max\ t_{gate}$) from d, the capacitance can be reduced, thus improving the bandwidth without affecting so much the modulation efficiency.

Observing the modulator schematic in Fig. 1, the poly-Si region (in blue) has n-type doping and the silicon region (in red) has p-type doping. To decrease the waveguide loss and the electrical access resistance between the RF signal and the waveguide, the modulator was designed with three doping levels (n/p, n_+/p_+, and n_{++}/p_{++}). The concentration level becomes higher when the colors (blue and red) become darker. The doping concentrations levels were symmetrical between the n-type and the p-type, for each region with the corresponding color level.

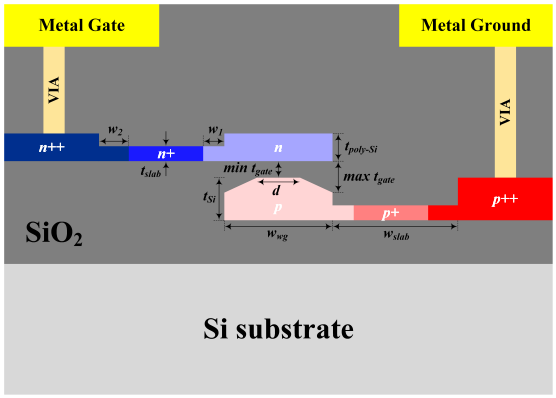

Fig. 1. Cross section view of the capacitive modulator with V-shaped gate thickness proposed.

Due to the complexity and limitation of the poly-Si parameters in the literature, silicon parameters were used for the top and bottom regions of the waveguide. To verify the accuracy of our simulation, a parallel study was performed and the results were validated according to two devices, as shown in Table I.

Table II describes the waveguide parameters used to design the modulator. The non-fixed parameters were used to optimize the device in several approaches, and they are represented by a range of values. The fixed parameters were scaled according to the specifications of most SOI platforms. The n/p doping was chosen based on our previous study [9], which shows an efficient agreement for low optical loss. Moreover, by setting n/p concentration, we will see in section IV-B that the $V_\pi \times L$ level can be adjusted by means of d and $max\ t_{gate}$ parameters.

TABLE I. Validation of results.

Year		2015		2019	
Waveguide architecture		Conventional poly-Si		Hybrid	
Ref.		[11]	Our results	[12]	Our results
$V_\pi \times L$	[V.cm]	0.48	0.5	1.3	1.25
$Loss$	[dB/mm]	0.97	∼1	2	1.4
C_{gate}	[fF/μm]	-	2.2	∼0.98	0.86

TABLE II. Optical simulation parameters.

Parameter	Description	Value	Unit
t_{Si}	Silicon waveguide thickness	220	[nm]
$t_{poly-Si}$	Poly-Si waveguide thickness	160	[nm]
t_{slab}	Slab thickness	70	[nm]
$min\ t_{gate}$	Minimum gate thickness	5	[nm]
$max\ t_{gate}$	Maximum gate thickness	10 to 100	[nm]
w_{wg}	Waveguide width	300 to 700	[nm]
w_{slab}	Slab width	1475	[nm]
w_1	Slab width with n/p doping	0 to 800	[nm]
w_2	Slab width with n_{++}/p_{++} doping	200	[nm]
d	Constant gate width	5 to 100	[nm]
n/p	n/p concentration	5×10^{17}	[cm^{-3}]
n_+/p_+	n_+/p_+ concentration	1×10^{19}	[cm^{-3}]
n_{++}/p_{++}	n_{++}/p_{++} concentration	1×10^{20}	[cm^{-3}]

During the simulation, a study of w_1 was performed to optimize the trade-off between optical insertion loss and electro-optical modulation bandwidth (related to electrical access resistance). For the electrical charges simulation, bias voltages from 0 to -5 V were applied on the metal gate, while 0 V was kept fixed on the metal ground (see Fig. 1). The homogeneous doping profile was considered for all charge carrier concentration levels.

Finally, all optical and charge simulations were performed using commercial Lumerical products. The analytical model for the electro-optical bandwidth calculation was implemented in commercial HFSS and Matlab softwares.

III. Modal Analysis

To design the modulator, it is necessary to adjust the waveguide width (w_{wg}) so that the device operates with a single propagation mode. For this, we need to know the modes characteristics that propagate through the waveguide. The first step is to sweep the waveguide width from 300 nm to 700 nm. The results, shown in Fig. 2, indicate that, during the w_{wg} sweep, four modes are found in the structure. Analyzing the effective index (n_{eff}), we noticed that the fundamental TE mode is highlighted in blue. Therefore, to choose the ideal waveguide width, the w_{wg} value must be in the range of 300

to 400 nm, since only the fundamental TE mode propagates. Values above 400 nm can provide unwanted modes, such as TE_1 and TE_2.

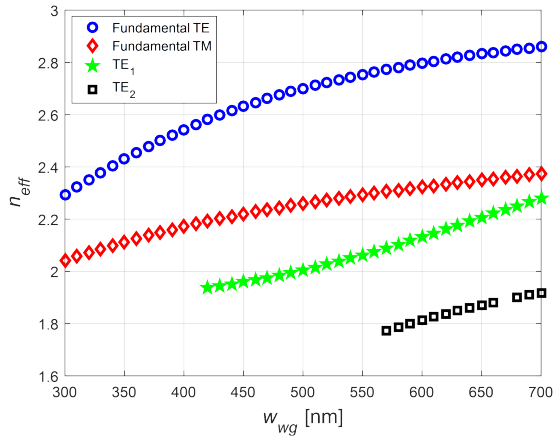

Fig. 2. Effective index when the waveguide width (w_{wg}) is swept from 300 to 700 nm.

Capacitive modulators are limited by the waveguide width. For a wide-waveguide (w_{wg} > 500 nm), the optical mode will be perfectly confined, but the device will be limited in speed, since the active area of the capacitor will be wider. Therefore, we need a shorter w_{wg} to provide a single propagation mode and high speed. In Fig. 1, we can observe a partial etching on the poly-Si region. During the simulations, we noted that, if the capacitive modulator with a short waveguide width (w_{wg} = 400 nm) has no etching on the poly-Si area, the optical mode scatters towards the high doping region (n_+), as shown in Fig. 3a. Thus, the optical mode is poorly confined, reducing the modulation efficiency. On the other hand, the partial etching presence confines the optical mode (see Fig. 3b) at the waveguide center, resulting in an improved modulation efficiency. With the etching strategy, we ensure a short active area device (high speed) with high optical confinement, without compromising the modulator performance.

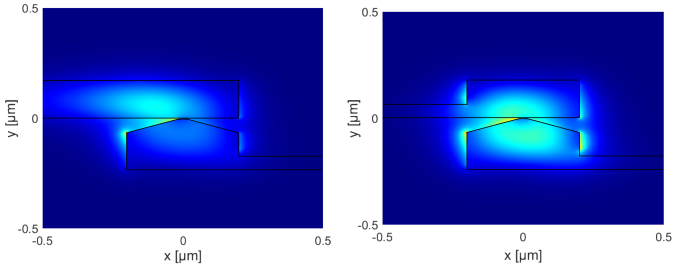

Fig. 3. TE-mode optical profile (a) without partial etching on the poly-Si and (b) with partial etching on the poly-Si, for w_{wg} = 400 nm.

According to the modal analysis presented in this section, from this point, w_{wg} is set to 400 nm.

IV. $V_\pi \times L$ and Loss Calculations

After the modal analysis, the next step is to calculate the modulation efficiency and optical loss as function of the voltage applied to the modulator. For this, the charge distribution for several applied voltages were calculated using a numerical software. Then, the charge mesh profile was saved and transferred to a modal solver. Finally, the refractive index change (Δn) and the absorption change ($\Delta\alpha$) were calculated using Soref and Bennett equations [13] for 1.55 μm wavelength,

$$\Delta n(x,y) = -8.8\times10^{-22}N_e(x,y) - 8.5\times10^{-18}N_h^{0.8}(x,y) \quad (1)$$

$$\Delta\alpha(x,y) = 8.5\times10^{-18}N_e(x,y) + 6.0\times10^{-18}N_h(x,y) \quad (2)$$

where N_e and N_h are the electrons and holes doping concentrations, respectively. Fig. 4 shows the carrier distribution for two voltages. It can be seen that, as expected, the charge concentration increases by several orders of magnitudes near the oxide gap.

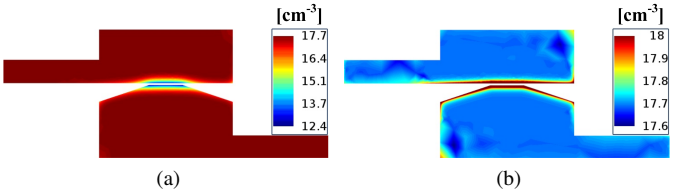

Fig. 4. Total carrier distribution for (a) V_{bias} = 0 V and (b) V_{bias} = -1.6 V. The concentration bars are in logarithmic scale.

The effective index can be calculated according to (4) [14]:

$$n(x,y) = n_{Si} + \Delta n(x,y) \quad (3)$$

$$n_{eff} = \frac{\iint_\infty n(x,y)|E(x,y)|^2 ds}{\iint_\infty |E(x,y)|^2 ds} \quad (4)$$

where $E(x,y)$ is the fundamental mode electric field distribution and n_{Si} is the silicon refractive index.

Based on the imaginary part of the effective index ($Im[n_{eff}]$), the mode optical loss, given in dB/m, is calculated according to (5).

$$Loss = -20\log_{10}\left(e^{-Im[n_{eff}]2\pi/\lambda_0}\right)\Big|_{\lambda_0=1.55\ \mu m} \quad (5)$$

An important figure of merit to evaluate the performance of silicon photonics modulators is the modulation efficiency ($V_\pi \times L$), given in V.m. Due to nonlinear change of the Si refractive index when subjected to a voltage, the $V_\pi \times L$ value also varies non-linearly regarding the bias voltage. According to [15], the product can be calculated as:

$$V_\pi \times L = \frac{\lambda_0}{2}\frac{dV_{bias}}{dn_{eff}}\Big|_{\lambda_0=1.55\ \mu m} \quad (6)$$

where V_{bias} is the reverse bias voltage.

A. Doping Width Optimization

At this point, the optical loss as function of the n/p doping width (w_1) was evaluated. With respect to this parameter (see Fig. 1), there is a trade-off between optical loss and bandwidth. If the high n_+/p_+ doping level is too close to the waveguide (short w_1), the optical loss will increase. However, the electrical access resistance will be lower, which improves the device bandwidth. To optimize this trade-off, the width w_1 was swept from 0 to 800 nm. It was verified that for w_1 values higher than 300 nm, the optical loss does not decreases significantly. Therefore, this value was chosen to minimize optical loss.

B. Analysis of d and $max\ t_{gate}$

This section discusses the modulator performance in several design scenarios. For this, d was swept from 5 to 100 nm and $max\ t_{gate}$ was swept from 10 to 100 nm, as shown in Fig. 5.

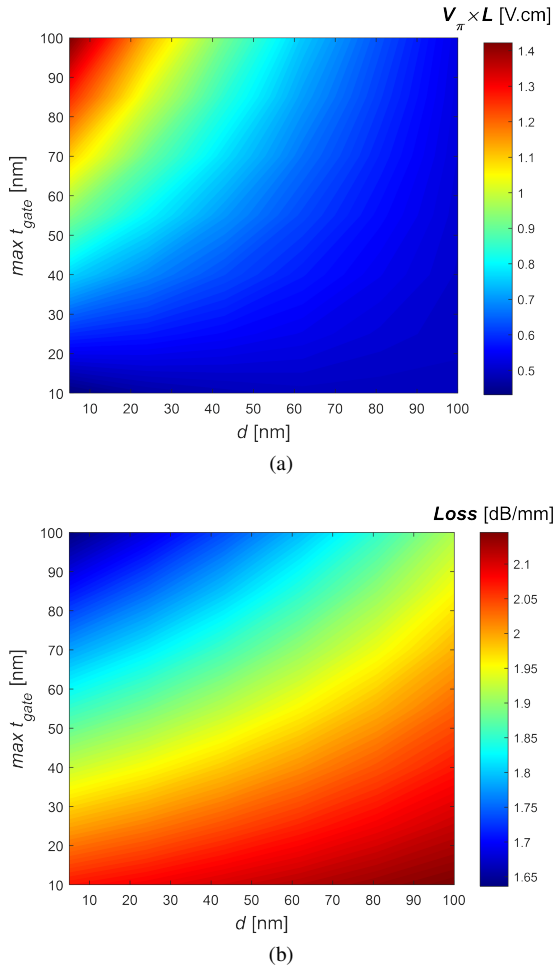

Fig. 5. (a) Modulation efficiency and (b) Optical loss in several design scenarios, for V_{bias} = -2 V.

In Fig. 5 it is possible to observe the trade-off between modulation efficiency and optical loss. Furthermore, it is noted that lower $max\ t_{gate}$ values combined with higher d values are required for the device to operate with lower $V_\pi \times L$.

To improve the modulation efficiency, it is important to verify the impact of the reverse bias voltage applied to the device. Fig. 6 shows the modulator performance when subjected to several voltages. In this analysis, the $max\ t_{gate}$ thickness was set to 100 nm (to provide high bandwidth).

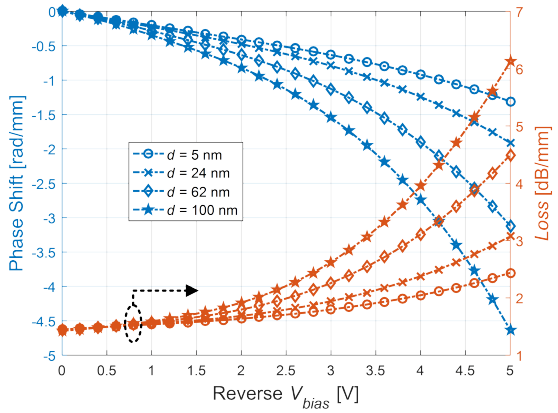

Fig. 6. Phase shift and its corresponding optical loss for several reverse bias voltages, when $max\ t_{gate}$ = 100 nm.

Fig. 6 shows that, by increasing the bias voltage from 0 to -5 V, the phase shift variation increase as the value of d increases. As the device must provide the highest modulation efficiency, we must consider higher V_{bias} combined with higher d parameter. For these scenarios, the optical loss can increase up to ∼6 dB/mm. However, in the case of lumped-type modulators, the total insertion loss can be considered relatively low, since the device length (L_{wg}) is typically < 1 mm. In this case, for a wide constant gate width (e.g. d = 100 nm, L_{wg} = 500 μm, and V_{bias} = -5 V), the optical insertion loss is acceptable (3 dB), corresponding to only $V_\pi \simeq 1$ V.

We have evaluated the connection loss from a standard waveguide to the modulator, using a linear taper. In this case, the results showed that, in order to reach maximum optical transmission (T $\simeq$ 98%), the access taper must be adjusted with a length of 115 μm, resulting in a coupling loss of ∼0.1 dB.

In this section, the $V_\pi \times L$ and loss trade-off was analyzed as function of some device's parameters. The next step is to analyze the electro-optical bandwidth in the same sweep parameters. In this way, some design scenarios will be explored to optimize the trade-off between bandwidth and V_π.

V. Bandwidth Analysis

This section presents a complete small-signal RF analysis to estimate the modulation bandwidth. Fig. 7 shows the device design with its equivalent electrical circuit.

A. Capacitance Analysis

The SiO_2 gate capacitance (C_{gate}) is calculated using the numerical derivative:

$$C_{gate} = \left.\frac{dQ}{dV}\right|_{V=V_{bias}} \tag{7}$$

where Q is the electrical charge. In this method, the total SiO_2 gate charge is automatically calculated by the electric

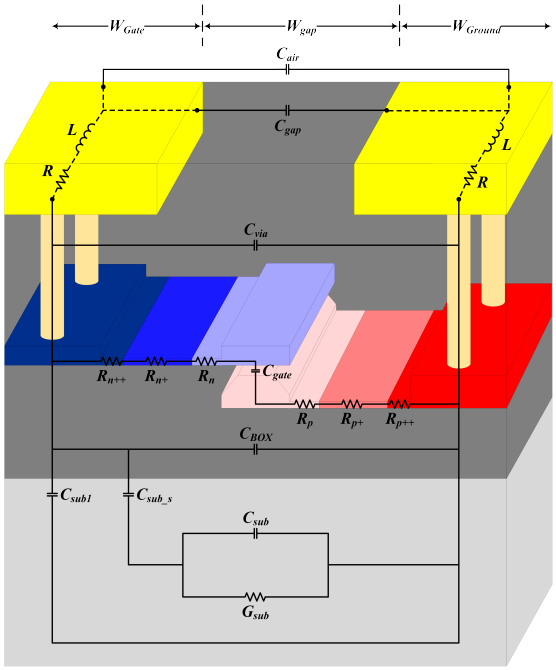

Fig. 7. 3D view of the modulator with its equivalent electrical circuit.

field monitor. During the calculation, the monitor integrates the electric field over its surface and uses Gauss's law to determine the net charge included within its volume.

Fig. 8 shows the capacitance behavior as function of the design parameters, when V_{bias} is equal to -5 V (to provide low V_π).

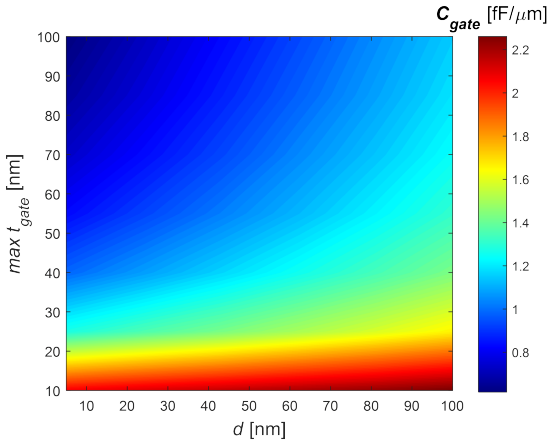

Fig. 8. Capacitance per unit length as function of d and $max\ t_{gate}$, for V_{bias} = -5 V.

In Fig. 8, the capacitance level increases as d increases. Thus, to design the device with higher bandwidth, it is necessary to take lower d combined with higher $max\ t_{gate}$ values. This scenario negatively affects the modulation efficiency, as seen in section IV-B. Therefore, in the next section, we will present some different design scenarios to explore this trade-off.

B. Transmission Line Modeling

For lumped-type modulators, the voltage is considered instantaneously uniform along the electrodes. In this way, the transmission line parameters, i.e. the inductance (L) and resistance (R) as a function of the operation frequency, were calculated according to the coplanar waveguide (CPW) model proposed by Heinrich [16]. In this approach, the capacitances and electrical conductance shown in Fig. 7 were calculated according to [17]. By using a numerical software for RF analysis (HFSS), the same calculations were performed to verify the accuracy of the Heinrich [16] model. For this, the CPW was considered unloaded and the transmission line parameters (Z, Y, and S) were calculated. Next, the transmission line parameters and the waveguide electrical components (R_{slabs} and C_{gate}) were included via MATLAB to form the modulator circuit. The slabs resistances (R_{slabs}) were obtained by numerical software using Ohm's law. Finally, the analytical model described in [14] was applied, which uses the RF transmission coefficient (accounting the impedance mismatch) and the system transfer function.

In Fig. 9, the equivalent electrical circuit was divided according to each corresponding part of the modulator. In addition, to facilitate the transfer function (H) calculation (ratio between the voltage on SiO_2 gate and the input voltage), three equivalent circuit loads were considered (Z_I, Z_{II}, and Z_{III}), which can be obtained from (8) to (13).

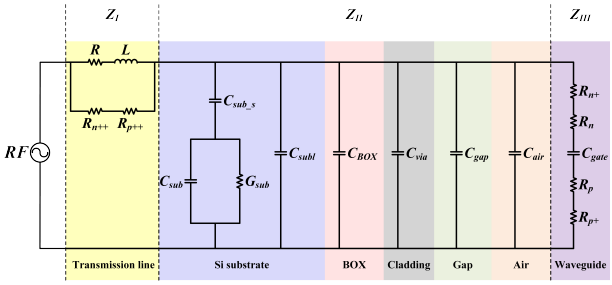

Fig. 9. Modulator circuit model.

$$Z_I = \frac{(R + jwL)(R_{n_{++}} + R_{p_{++}})}{R + R_{n_{++}} + R_{p_{++}} + jwL} \tag{8}$$

$$Z_{II}^A = \frac{jwC_{sub\_s}(jwC_{sub} + G_{sub})}{jw(C_{sub} + C_{sub\_s}) + G_{sub}} \tag{9}$$

$$Z_{II}^B = jw(C_{subl} + C_{BOX} + C_{via} + C_{gap} + C_{air}) \tag{10}$$

$$Z_{II} = (Z_{II}^A + Z_{II}^B)^{-1} \tag{11}$$

$$R_{slabs} = R_n + R_{n_+} + R_p + R_{p_+} \tag{12}$$

$$Z_{III} = (jwC_{gate}R_{slabs} + 1)(jwC_{gate})^{-1} \tag{13}$$

$$H_A = [Z_I(jwC_{gate}R_{slabs} + 1)]^{-1} \tag{14}$$

$$H_B = Z_I^{-1} + Z_{II}^{-1} + Z_{III}^{-1} \tag{15}$$

$$H = H_A H_B^{-1} \tag{16}$$

The RF voltage transmission can be written as:

$$\Gamma = 2Z_L(Z_L + Z_0)^{-1} \tag{17}$$

where Z_L represents the equivalent load $(Z_I + Z_{II}||Z_{III})$, Z_0 is the input characteristic impedance and ω is the angular frequency of the electric signal.

Finally, the electro-optical response, in dB, can be written as:

$$S_{21} = 20\log_{10}|\Gamma \times H| \tag{18}$$

In order to provide higher bandwidth, the input characteristic impedance was set to Z_0 = 5 Ω, as proposed in [18]. A sweep in the electrode parameters (W_{Gate} and W_{gap}) was made in order to find the best values to maximize the electro-optical bandwidth. The results were W_{Gate} = 40 μm and W_{gap} = 65 μm, and they were the same for all waveguide geometries considered.

C. Electro-Optical Bandwidth Analysis

After the transmission line modeling discussed in section V-B, the electro-optical bandwidth results will be analyzed. Fig. 10 shows the bandwidth as function of the waveguide parameters, when L_{wg} = 250 μm.

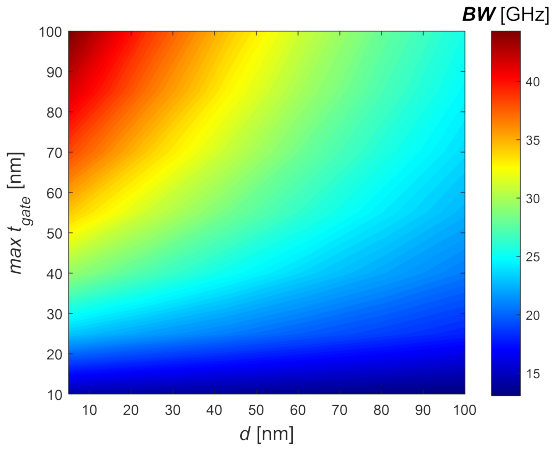

Fig. 10. Electro-optical bandwidth as function of d and $max\ t_{gate}$, for V_{bias} = -5 V and L_{wg} = 250 μm.

Note that, contrary to the V_π behavior, the modulator achieves maximum bandwidth in cases of minimum d and maximum $max\ t_{gate}$. However, the proposed waveguide structure allows the bandwidth to be sacrificed for high d values, since this architecture has resulted in high BW levels.

In order to verify the accuracy of the methods used in the transmission line modeling, Fig. 11 compares the electro-optical response between the simulated model proposed by Heinrich [16] and the HFSS software. In Fig. 11 the estimated bandwidth between the two approaches are similar, presenting 4% average relative error. This shows that the analytical model can be used, resulting in much less computational effort.

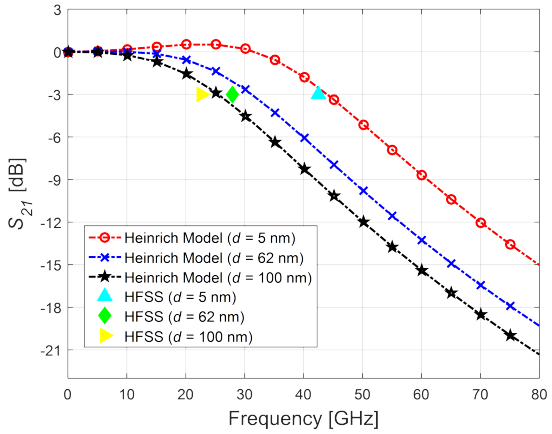

Fig. 11. Electro-optical response for V_{bias} = -5 V, $max\ t_{gate}$ = 100 nm, and L_{wg} = 250 μm.

D. Dynamic OMA Analysis

In the previous sections, the modulation efficiency, loss, and bandwidth were analyzed in detail in several scenarios. In this section, the maximum dynamic optical modulation amplitude (OMA), which evaluates the systemic performance of the device, was analyzed based on the main modulator parameters, d and $max\ t_{gate}$. For this, the ideal OMA level that the device can offer for a symbol rate of 56 Gbaud was calculated according to the optimal active length, as proposed in [19]. Fig. 12 shows this analysis for two modulation formats, OOK and PAM-4.

For OOK format, the best OMA (-2.63 dBm) is set in the parameters d = 62 nm, $max\ t_{gate}$ = 70 nm, and L_{wg} = 248.7 μm. On the other hand, the maximum PAM-4 OMA (-7.69 dBm) is reached when d = 5 nm, $max\ t_{gate}$ = 100 nm, and L_{wg} = 184.4 μm. This range of values are comparable to the ones presented in [19].

VI. Waveguide Manufacturing Feasibility

Traditionally, in order to etch the silicon waveguide with an angle with respect to the etch direction, the use of anisotropic wet etching with KOH is used [20]. However, the etching angle is fixed to the silicon molecules crystalline direction, which is about 54.7°, therefore it is not suitable for fabricating the proposed device. An alternative is to use the ion beam etching (or milling), as reported in [21], which is achieved by directing a beam of charged particles (ions) at a substrate with a suitably patterned mask in a high vacuum chamber. Another alternative, which is claimed to be less expensive, is to use plasma etching with the aid of a Faraday cage [22], [23]. In the conventional plasma etching technique, the direction of the etching ions is always vertical to the etched surface because of the electric-field that is formed in the substrate surface. Because of that, the etching is anisotropic even if the substrate is tilted with respect to the ion direction. As proposed in [22], [23], the use of the Faraday cage makes the electric potential uniform

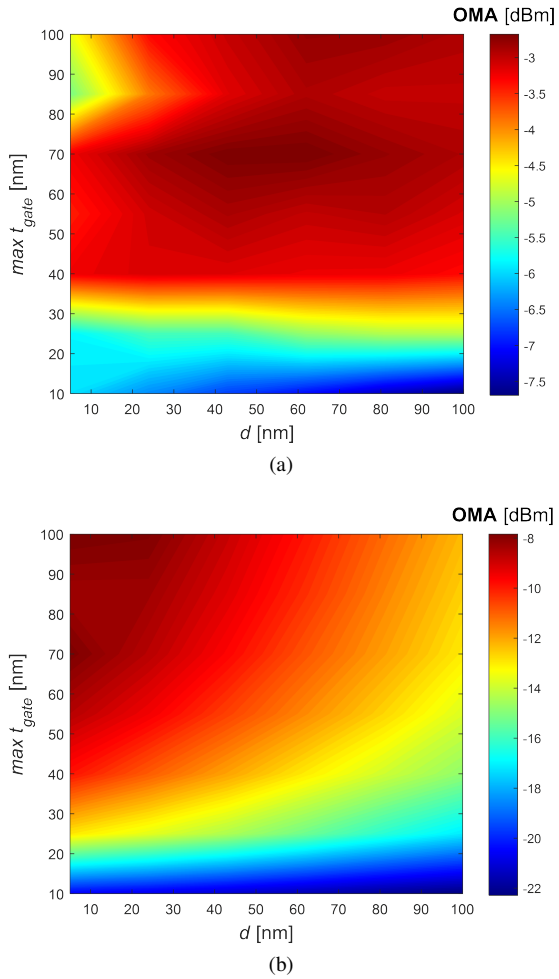

Fig. 12. Maximum dynamic OMA for (a) OOK and (b) PAM-4 modulation formats, when V_{bias} = -5 V with V_{pp} = 4 V.

inside it. In this way, the etching direction can be controlled by the substrate place holder angle. Therefore, the Faraday cage etching method is a potential approach for future manufacture of the V-shaped oxide gate modulator proposed in this paper.

VII. Conclusion

In this paper we propose a silicon modulator configuration to improve the trade-off between V_π and bandwidth. The architecture is based on a capacitive device, which uses the carrier accumulation mechanism. Trade-offs between optical loss, modulation efficiency and bandwidth are analyzed with respect to a set of physical parameters. A study of the waveguide geometry was performed, showing that the device should be designed with short width (w_{wg} = 400 nm) for single TE-mode and high bandwidth operation. In addition, to improve the optical confinement, a partial etching on the poly-Si region is proposed.

For a better comparison, a study of recent references based on capacitive lumped-type modulators was performed. Table III shows the results where we propose design solutions (d and $max\ t_{gate}$) of V-shaped SiO_2 gate modulators in the same length (L_{wg}) conditions that were assigned in the references.

TABLE III. State-of-the-art references and V-shaped SiO_2 gate modulators.

State-of-the-art references						
Ref.		[24]	[25]	[26]	[27]	[12]
Year		2017	2017	2018	2018	2019
Waveguide architecture		Hybrid	Hybrid	Vertical SiO_2	Hybrid	Hybrid
V_{bias}	[V]	1	-3	3	4	4
L_{wg}	[μm]	500	250	500	250	250
t_{gate}	[nm]	5	10	14	20	20
V_π	[V]	0.86	3.5	30.6	40	52
$Loss$	[dB]	0.95	~1	2.5	0.5	0.5
C_{gate}	[fF]	~3000	-	~450	>350	>245
BW	[GHz]	~0.1	<2.2	<42	>25	30
V-shaped SiO_2 gate modulators @ -5 V						
L_{wg}	[μm]	500	250	500	250	250
$max\ t_{gate}$	[nm]	100	100	100	100	100
d	[nm]	100	100	5	62	24
V_π	[V]	~1	2.2	12.8	5.7	14.2
$Loss$	[dB]	3	1.5	1.2	1.1	0.77
C_{gate}	[fF]	575	287.5	305	232.5	180
BW	[GHz]	20.4	25.6	30.3	~31	~39

Observing the state-of-the-art results (top of the Table III), it is noted that devices with lower V_π have insignificant bandwidth. On the other hand, the modulator presented in this work (bottom of the Table III) present a better trade-off, since lower C_{gate} capacitances were obtained to provide higher bandwidths, without reducing significantly the V_π. Finally, the results compared with state-of-the-art references show advantages with respect to V_π and bandwidth trade-off. In addition, an OMA analysis have shown that the device presents similar performance with other capacitive modulators [19]. In a future work, a deeper OMA analysis will be made, in order to assess the feasibility of the proposed device in an actual system transmission.

References

[1] PhotonicsPPP, "Photonics21 Research and Innovation topics (RIA) for the Horizon2020 PPP Work Programme 2018-2020," https://www.photonics21.org/download/about-us/photonics-ppp/photonics-ppp_research-and-innovation-topics.pdf?m=1513605489&, 2018, [Online; accessed 6-May-2019].

[2] R. C. Figueiredo, A. L. N. Souza, S. M. Ranzini, and A. Chiuchiarelli, *Multilevel Pulse Amplitude Modulation Transmissions for Data Center Applications*. Cham: Springer International Publishing, 2019, pp. 1–16.

[3] IMEC, "imec-ePIXfab SiPhotonics: iSiPP50G," http://www.europractice-ic.com/SiPhotonics_technology_imec_ISIPP50G.php, [Online; accessed 6-May-2019].

[4] D. J. Thomson, F. Y. Gardes, S. Liu, H. Porte, L. Zimmermann, J. Fedeli, Y. Hu, M. Nedeljkovic, X. Yang, P. Petropoulos, and G. Z. Mashanovich, "High Performance Mach–Zehnder-Based Silicon Optical Modulators," *IEEE Journal of Selected Topics in Quantum Electronics*, vol. 19, no. 6, pp. 85–94, Nov 2013.

[5] H. Xu, X. Li, X. Xiao, Z. Li, Y. Yu, and J. Yu, "Demonstration and Characterization of High-Speed Silicon Depletion-Mode Mach–Zehnder Modulators," *IEEE Journal of Selected Topics in Quantum Electronics*, vol. 20, no. 4, pp. 23–32, July 2014.

[6] D. Petousi, L. Zimmermann, A. Gajda, M. Kroh, K. Voigt, G. Winzer, B. Tillack, and K. Petermann, "Analysis of Optical and Electrical Trade-offs of Traveling-Wave Depletion-Type Si Mach–Zehnder Modulators for High-Speed Operation," *IEEE Journal of Selected Topics in Quantum Electronics*, vol. 21, no. 4, pp. 199–206, July 2015.

[7] E. El-Fiky, A. Samani, M. Sowailem, M. Osman, M. Jacques, D. Patel, M. G. Saber, L. Xu, Z. Xing, M. Xiang, and D. V. Plant, "Dual Parallel Multielectrode Traveling Wave Mach–Zehnder Modulator for 200 Gb/s Intra-datacenter Optical Interconnects," *IEEE Photonics Journal*, vol. 11, no. 1, pp. 1–9, Feb 2019.

[8] A. Liu, R. Jones, L. Liao, D. Samara-Rubio, D. Rubin, O. Cohen, R. Nicolaescu, and M. Paniccia, "A high-speed silicon optical modulator based on a metal-oxide-semiconductor capacitor," *Nature*, vol. 427, pp. 615–618, Feb 2004.

[9] D. M. Dourado, M. L. Rocha, J. P. P. Carmo, G. B. Farias, and J. E. Ribeiro, "Modeling and trade-off analysis of a capacitive silicon Mach-Zehnder modulator for telecom applications," in *2018 SBFoton International Optics and Photonics Conference (SBFoton IOPC)*, Oct 2018, pp. 1–5.

[10] K. Shastri, P. Gothoskar, M. Ghiron, V. Patel, R. K. Montgomery, S. Pathak, and K. A. Yanushefski, "High Speed, Silicon-Based Electro-Optic Modulator," Jun. 20 2006, patent US 7,065,301 B2.

[11] S. Zhu and G. Lo, "Designs of Silicon MIS Phase Modulator With a Deposited AlN Film as the Gate Dielectric," *IEEE Photonics Technology Letters*, vol. 27, no. 11, pp. 1236–1239, June 2015.

[12] T. Thiessen, P. Grosse, J. D. Fonseca, P. Billondeau, B. Szelag, C. Jany, J. k. S. Poon, and S. Menezo, "30 GHz heterogeneously integrated capacitive InP-on-Si Mach–Zehnder modulators," *Opt. Express*, vol. 27, no. 1, pp. 102–109, Jan 2019.

[13] R. Soref and B. Bennett, "Electrooptical effects in silicon," *IEEE Journal of Quantum Electronics*, vol. 23, no. 1, pp. 123–129, January 1987.

[14] X. Li, F. Yang, F. Zhong, Q. Deng, J. Michel, and Z. Zhou, "Single-drive high-speed lumped depletion-type modulators toward 10 fJ/bit energy consumption," *Photon. Res.*, vol. 5, no. 2, pp. 134–142, Apr 2017.

[15] Y. Zhou, L. Zhou, H. Zhu, C. Wong, Y. Wen, L. Liu, X. Li, and J. Chen, "Modeling and optimization of a single-drive push-pull silicon Mach-Zehnder modulator," *Photon. Res.*, vol. 4, no. 4, pp. 153–161, Aug 2016.

[16] W. Heinrich, "Quasi-TEM description of MMIC coplanar lines including conductor-loss effects," *IEEE Transactions on Microwave Theory and Techniques*, vol. 41, no. 1, pp. 45–52, Jan 1993.

[17] H. Yu and W. Bogaerts, "An Equivalent Circuit Model of the Traveling Wave Electrode for Carrier-Depletion-Based Silicon Optical Modulators," *Journal of Lightwave Technology*, vol. 30, no. 11, pp. 1602–1609, June 2012.

[18] S. Zhou, H. ta Wu, K. Sadeghipour, C. Scarcella, C. Eason, M. Rensing, M. J. Power, C. Antony, P. O'Brien, P. D. Townsend, and P. Ossieur, "Optimization of PAM-4 transmitters based on lumped silicon photonic MZMs for high-speed short-reach optical links," *Opt. Express*, vol. 25, no. 4, pp. 4312–4325, Feb 2017.

[19] F. Boeuf, J. Han, S. Takagi, and M. Takenaka, "Benchmarking Si, SiGe, and III–V/Si Hybrid SIS Optical Modulators for Datacenter Applications," *Journal of Lightwave Technology*, vol. 35, no. 18, pp. 4047–4055, Sep. 2017.

[20] M. J. Madou, *Fundamentals of Microfabrication: The Science of Miniaturization*, 2nd ed. CRC Press, March 2002.

[21] J. M. E. Harper, J. J. Cuomo, P. A. Leary, G. M. Summa, H. R. Kaufman, and F. J. Bresnock, "Low energy ion beam etching," *J. Electrochem. Soc.*, vol. 128, no. 5, pp. 1077–1083, January 1981.

[22] J.-H. Kim, S.-W. Cho, and C.-K. Kim, "Fabrication of Slanted Nanostructures Using a Faraday Cage System," in *2015 14th International Conference on Non-Linear Analysis, Non-Linear Systems and Chaos (NOLASC '15) and 6th International Conference on Nanotechnology (NANOTECHNOLOGY '15)*, Nov 2015, pp. 126–129.

[23] P. Latawiec, M. J. Burek, Y.-I. Sohn, and M. Loncar, "Faraday cage angled-etching of nanostructures in bulk dielectrics," *J. Vac. Sci. Technol. B*, vol. 34, no. 4, pp. 041 801.1–041 801.7, March 2016.

[24] J.-H. Han, F. Boeuf, J. Fujikata, S. Takahashi, S. Takagi, and M. Takenaka, "Efficient low-loss InGaAsP/Si hybrid MOS optical modulator," *Nature Photonics*, vol. 11, pp. 486–491, Jul 2017.

[25] T. Hiraki, T. Aihara, K. Hasebe, K. Takeda, T. Fujii, T. Kakitsuka, T. Tsuchizawa, H. Fukuda, and S. Matsuo, "Heterogeneously integrated III-V/Si MOS capacitor Mach-Zehnder modulator," *Nature Photonics*, vol. 11, pp. 482–486, Jul 2017.

[26] K. Debnath, D. J. Thomson, W. Zhang, A. Z. Khokhar, C. Littlejohns, J. Byers, L. Mastronardi, M. K. Husain, K. Ibukuro, F. Y. Gardes, G. T. Reed, and S. Saito, "All-silicon carrier accumulation modulator based on a lateral metal-oxide-semiconductor capacitor," *Photonics Research*, vol. 6, no. 5, pp. 373–379, May 2018.

[27] S. Menezo, T. Thiessen, P. Grosse, J. K. S. Poon, C. Jany, J. D. Fonseca, B. Szelag, B. Charbonnier, G. El-Zammar, O. Lemonnier, P. Bilondeau, S. Malhouitre, B. Montmayeul, and L. Sanchez, "High-Speed Heterogeneous InP-on-Si Capacitive Phase Modulators," in *2018 Optical Fiber Communications Conference and Exposition (OFC)*, March 2018, pp. 1–3.

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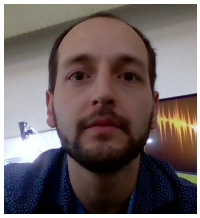

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