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Low-power/low-voltage RF microsystems for wireless sensors networks

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ABSTRACT

This paper presents radio-frequency (RF) microsystems (MSTs) composed by low-power devices for use in wireless sensors networks (WSNs). The RF CMOS transceiver is the main electronic system and its power consumption is a critical issue. Two RF CMOS transceivers with low-power and low-voltage supply were fabricated to operate in the 2.4 and 5.7 GHz ISM bands. The measurements made in the RF CMOS transceiver at 2.4 GHz, which showed a sensitivity of −60 dBm with a power consumption of 6.3 mW from 1.8 V supply. The measurements also showed that the transmitter delivers an output power of 0 dBm with a power consumption of 11.2 mW. The RF CMOS transceiver at 5.7 GHz has a total power consumption of 23 mW. The target application of these RF CMOS transceivers is for MSTs integration and for use as low-power nodes in WSNs to work during large periods of time without human operation, management and maintenance. These RF CMOS transceivers are also suitable for integration in thermoelectric energy scavenging MSTs.

1. Introduction

Wireless communication microsystems (MSTs) with high density of nodes and simple protocol are emerging for low-data-rate distributed sensor network applications such as those in home automation and industrial control. This type of wireless microsystems with sensors and electronics is also becoming of interest for biomedical applications. Thus, in order to implement an efficient power-consumption wireless sensor node, it is necessary to develop low-power/low-voltage radio-frequency (RF) transceivers.

After more than two decades of relentless scaling to ever smaller dimensions for higher packing density, faster circuit speed, and lower power dissipation, CMOS technology has become today's prevailing technology [1]. These advances led the design engineers to extensively develop RF circuits in CMOS technology with a low cost. The selection of the most suitable CMOS process to fabricate RF devices plays an important role because despite the technology tradeoffs, the specifications must be met. Thus, the generally proven and accepted fact that as the MOSFET channel length is scaled down, power supply voltage is reduced as well to keep active power and electric field (reliability) within reasonable limits constitutes a valuable knowledge on the design of RF devices [1]. This paper presents low-power wireless microsystems for use in wireless sensors networks with two frequencies of the ISM band: the 2.4 and the 5.7 GHz. Two RF CMOS transceivers for operation at the frequencies of 2.4 and 5.7 GHz were optimized and fabricated in the UMC 0.18 μm RF CMOS process to have low power consumptions with a power supply of 1.8 V. Anti-electrostatic discharge (anti-ESD) protections must be included in CMOS devices to avoid their destruction or malfunction. However, anti-ESD protections can drastically change the behaviour of RF circuits, e.g., the increase of mismatchings between antennas and Low-Noise Amplifiers (LNA). Thus, in order to minimize the impact of the anti-ESD protections, compensation techniques must be provided. This paper presents, for the RF CMOS transceiver at 2.4 GHz, a set of compensation techniques with useful guidelines that can be successfully applied in other RF designs.

The design of a low-power transmitter is different of an energy efficient transmitter. The lifetime maximization of a battery is achieved, if the design is focused to minimize the power consumption rather than the power dissipation. Both RF CMOS transceivers offer the possibility to control the power during the transmission; at the same time it is possible to select which subsystem is to be enabled or disabled. This last function of RF CMOS transceivers make them suitable for integration in MSTs where the control and processing blocks are only responsible for activating the wireless communications. The two power goals formerly cited are targeted with the use of these two RF CMOS transceivers. Moreover, when compared with commercial devices, the possibility to be integrated with the sensors in the same MST is another competitive advantage of these RF CMOS transceivers.

2. System requirements

In wireless sensor networks, the communication is made by way of an RF link. Thus, in order to make such a communication possible, a wireless interface must be designed. A wireless interface is an RF CMOS transceiver, which, after being connected to an associated antenna, allows wireless communications with the exterior. A wireless microsystem can include an RF CMOS transceiver, sensors and electronics of processing and control. The size of the RF CMOS transceiver must be comparable with those found in the other elements of a microsystem, in order to produce miniaturized microsystems with the smallest dimensions (for allowing the mass production at low prices). Moreover, wireless microsystems can have great flexibility. This means that it is possible to select how many and which type of sensors, what type of RF CMOS transceiver and what electronics can integrate the microsystem. In conclusion, wireless microsystems can be available for a huge range of applications, using multi-chip-module (MCM) techniques.

In wireless communications, the antenna is one of the most critical subsystems and must be small enough to comply with the size constraints of the microsystems, in order not to compromise the desired miniaturization. This means that the key solution to achieve a fully integrated solution is the research of new frequency bands [2] and new geometries [3] in order to fabricate smaller antennas for integration in wireless microsystems [4,5]. The dimension of an antenna is proportional to the operating wavelength. Thus, the migration of wireless communication systems to higher frequency bands (as it is the case of the 5–6 GHz ISM band) facilitates on-chip implementation of antennas [3]. Thus, the selection of the frequency is one of the more important design aspects. Normally, the frequency must take in account some key aspects: the desired range, the baud rate and the power consumption. Unfortunately, these aspects trade between them, i.e., the optimization of one affects the others in an opposite way. The attenuation of RF signals in the free-space increases with distance; thus, for a simultaneously given transmitted power, P_t (dB), and receiver's sensitivity, S_r (dB), the frequency of operation is limited by the range, d_{max} (m) [6]

$$f \leq 10^{((P_t - S_r) - 20\log_{10}(4\pi d_{max})/20)} \text{ (Hz)}. \quad (1)$$

An increase in the power of RF signals, P_t (dB), compensates the additional losses in the radiowave channel. However, an increase in the transmitted power implies a higher power consumption, whose consequence is a decrease in the useful life of the battery. In conclusion, increasing the transmitted power is an unacceptable solution, especially when the goal is to keep or even increase the life of batteries. Applications that need high baud rates also require high signal bandwidths. However, the frequency cannot be arbitrarily increased because of the severe implications in the power consumption. The problem is due to the transistors to switch faster, resulting in high-energy dissipations and power consumptions.

The available bands for wireless communications systems are summarized in Fig. 1. It is possible to use the standardized technologies, such as the Bluetooth [7], the ZigBee [8], the WLAN (IEEE) 802.11 [9] or the LR–WPAN (IEEE) 802.15.4 [10]. Additionally, it is possible to select proprietary solutions working with any one of the ISM bands (Industrial, Scientific and Medical). The ISM bands are unregulated frequencies not subjected to standardization that can be used without any specific authorization. The flexibility offered by the ISM bands to prototype user-specific wireless networks resulted in the widespread use of huge and interesting applications. Another wireless technology is the radio-frequency identification (RFID) that comprises two classes of operation: magnetic and electromagnetic field usage. The difference between them is in the type of field to exchange the information and to supply the RFID devices. It is also possible to explore optical approaches, using lasers in point-to-point links and standardized solutions supported by infra-red devices (IrDA).

3. Developed microsystems

3.1. Body motion monitoring at 2.4 GHz

Body motion monitoring of individuals is of major importance in bioengineering and rehabilitation [11]. Fig. 2(a) illustrates the block diagram and the respective interface for monitoring the body movements of individuals. Fig. 3(b) shows the wireless interface mounted in the arm of a test-dummy, which simulates the movements of patients. This system is an implementation of a real wireless interface for data acquisition and transmission using the wireless sensors network paradigm. Two accelerometers with three axes measure the relative position of members to the thorax. The acquired signals from the accelerometers are processed by a signal conditioning block and a second-order low-pass filter. This processed and filtered signal is further amplified, before sampling and analog-to-digital conversion (ADC). The analog electronics of

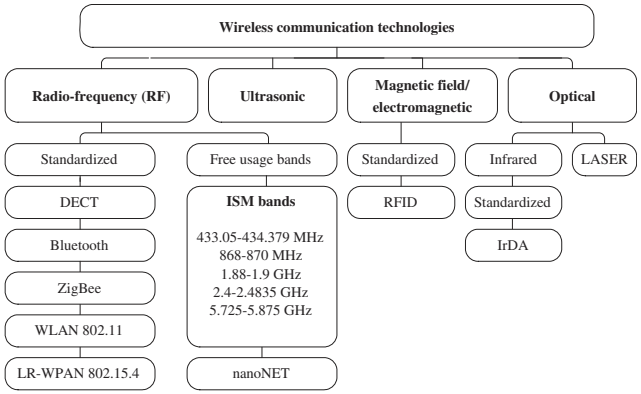

Fig. 1. Available frequency bands and respective applications.

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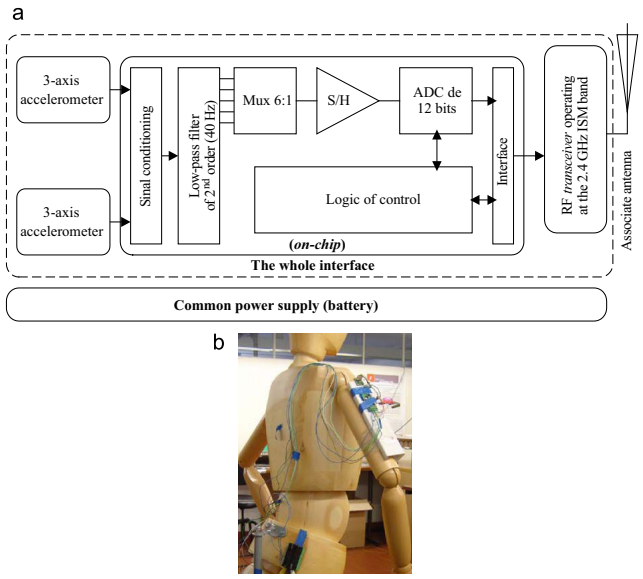

Fig. 2. (a) The block diagram of a wireless interface for operation at the 2.4 GHz ISM band and ready to be used in biomedical applications and (b) an interface already mounted in the arm of a test-dummy.

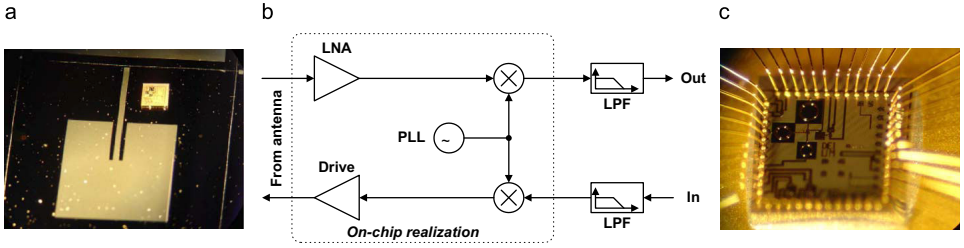

Fig. 3. (a) Chip-size antenna for operation at 5.7 GHz assembled with the RF CMOS transceiver, (b) the structure and (c) a photograph of the RF CMOS transceiver.

control and processing is managed using the control logic. The RF module uses a 2.4 GHz wireless link to exchange data.

3.2. Wireless microsystem with on-chip antenna at 5.7 GHz

The fabrication of chip-size antennas to be integrated in wireless microsystems is possible for frequencies at the range 5.7–5.89 GHz. Moreover, these antennas reduce the impedance mismatches problems; at the same time, they systematize the manufacturing processes and deliver microsystems with an even reduced price [12]. Fig. 3(a) shows a photograph of a microsystem with an RF CMOS transceiver mounted together with a chip-size antenna of planar type. The antenna was optimized and fabricated for operation in the 5.7 GHz ISM band and measures 7.6 × 7.7 mm [5]. Fig. 3(b) illustrates the block diagram of the RF CMOS transceiver at 5.7 GHz. This RF CMOS transceiver uses the ASK modulation to transmit the data. This RF CMOS transceiver was fabricated in the UMC 0.18 μm CMOS process because it trades the high-frequency capability of minimum-length transistors with low current consumption by biasing the devices at low current densities, even for devices working at RF. Also, this process provides a polysilicon and six metal layers, as well as integrated spiral inductors (with a quality factor of ten), high resistor values (a special layer is available) and it works with the low-power supply of 1.8 V. The microdevice shown in Fig. 3(c) is the RF CMOS transceiver at 5.7 GHz.

This RF CMOS transceiver has a Low-Noise Amplifier (LNA) that provides an input impedance of 50 Ω. The amplified RF signal is directly converted to the baseband with a single balanced active

CMOS mixer. The internal oscillator is a Phase-Locked Loop (PLL) working at 5.7 GHz. The transceiver is able to operate at the [5.42–5.83 GHz] frequency range. This is done by changing the frequency division ratio in the feedback path of the PLL. The PLL has four digital inputs for the division ratio programming. The output frequency is $f_{out}=f_{ref}\times 2(200+D)$, where D, with $D\in\{0, 1,\ldots, 15\}$, is the decimal representation of the division ratio. The used reference frequency was f_{ref}=13.56 MHz. The high power consumption of RF PLLs is mainly due to the first stages of the frequency divider that often dissipates half of the total power. The measurements show for the LNA a gain in the range [9.6–9.8 dB], a noise figure, NF, in the range [0.78–0.84 dB] and a stabilization factor K of 1.21 for making the LNA unconditionally stable ($K>1$). The power consumptions are: about 9.65 mW for the LNA, about 9.51 mW for the mixers and 4.14 mW for the PLL.

3.3. Low-power and power-efficient wireless microsystem at 2.4 GHz

In wireless sensors networks, the continuous working time of sensorial nodes is limited by its average power consumption [13]. In the wireless node and excluding the RF CMOS transceiver, the majority of the electronic devices do not have great impact in terms of power consumption [14]. In fact, it is well demonstrated that the RF CMOS transceiver is the subsystem with the high power consumption regardless of the increased availability of technologies with increased power-consumption efficiencies [15]. The definition of new architectures and algorithms are topics of increased concern in wireless microsystems. The main issue is to quantify in advance the exact implication of the RF transceiver in the total power consumption [16]. Thus, without proper design, the communication will increase network power consumption significantly because listening and emitting are power-intensive activities [17]. In order to optimize the power consumption, an RF CMOS transceiver was optimized and fabricated for operation in the 2.4 GHz ISM band. This new RF CMOS transceiver was fabricated in the same 0.18 μm CMOS process previously presented. Moreover, in order to optimize power management, the RF CMOS transceiver design predicts the use of control signals. These control signals allow one to enable and disable all the subsystems of the RF CMOS transceiver, e.g., to switch off the receiver when an RF signal is being transmitted or to switch off the transmitter when an RF signal is being received. Also it is possible to put the RF CMOS transceiver to sleep when RF signals are neither transmitted nor received. An important feature allowed by this RF CMOS transceiver is the possibility of being integrated together in the same microsystem with sensors and remain electronics of processing and control. This reduces the number of supply-points (Fig. 4), which makes it more practical and easy to supply all the subsystems with a single battery.

Fig. 5 shows the architecture of the RF CMOS transceiver, which is composed of a receiver, a transmitter, an RF switch and a Phase-locked Loop (PLL) that works as a frequency synthesizer.

The receiver's front-end is a chain composed of a Low-Noise Amplifier (LNA), a post-amplifier, an envelope detector and an output buffer. The post-amplifier provides additional gain to the RF signal at the output of the LNA and the envelope detector senses the presence or the absence of the 2.4 GHz carrier. Then, the signal provided at the output of the envelope detection is injected in the output buffer, which transforms it in a perfect NRZ (Non-Return to Zero) rail-to-rail signal.

The input block of the transmitter is a modulator circuit that generates a preliminary version of a digital ASK signal. The preliminary ASK signal is the result of a combination of the bitstream with a square wave of 2.4 GHz. The signal at the output of the modulator circuit is applied to a switched Power Amplifier (PA) and further filtered by an external filter. The filtered signal is the modulated ASK signal that is injected in the antenna for RF transmission. The PA allows the selection of the transmitted power. The local generated 2.4 GHz carrier is generated in a PLL. The PLL has a reference generator circuit with a crystal oscillator at 20 MHz, followed by a phase-frequency difference circuit (PFD), a current steering charge-pump (CP) and a third-order passive filter. The passive section output is connected to a Voltage-Controlled Oscillator (VCO) that generates the local carrier at 2.4 GHz. This frequency must be divided by 120 and connected to the PFD again, closing the loop.

An internal RF switch makes this transceiver a true complete system-on-a-chip (SOC). The RF switch connects the antenna to

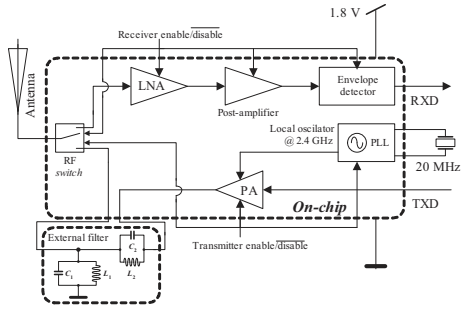

Fig. 5. The architecture of the low-power/low-voltage RF CMOS transceiver at 2.4 GHz.

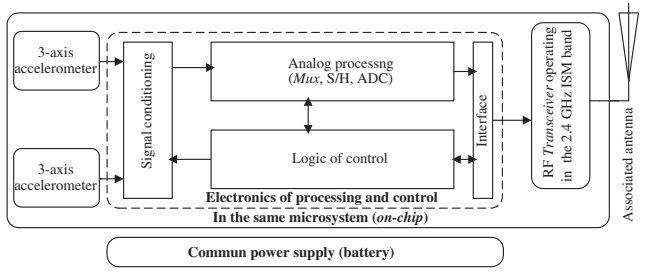

Fig. 4. A wireless microsystem that integrates the RF CMOS transceiver, sensors and electronics.

one of the receiver or transmitter path, which connects to the receiving and transmitting ports, respectively. The isolation between non-connected ports must be high. In order to have a power-efficient transceiver without degrading its sensitivity, the losses in the switch must be low.

The power budget of the RF link must guarantee that for any noise condition, the RF CMOS transceiver can exchange data at the maximum baud rate of 250 kbps with a bit error probability (BEP) less than 10^{-6} (BEP=$P_e \leq 10^{-6}$). This target quality of service (QoS) is for a maximum transmitted power of P_T=0 dBm (p_t=1 mW) with Amplitude Shift Keying (ASK) modulation. Several measurements of the environment noise were made, using an antenna with an output impedance of 50 Ω (at the frequency of 2.4 GHz) and a Spectrum Analyzer, model *Agilent E4404–B*. The observations revealed a noise power, N (dB), always below $N=-104$ dB. It is mandatory to obtain the full characterization of noise powers and to specify the QoS in order to obtain the minimum sensitivity of the receiver. In ASK transmission systems with envelope detection (also known as non-coherent ASK) the BEP is [18], $P_e=\frac{1}{2}e^{-\gamma_0/2}$, $\gamma_0 \gg 1$, where γ_0 is the signal-to-noise ratio (SNR) at the receiver. Thus, a minimum SNR of $\gamma_0 \geq 26$ ($\gamma_{0\,dB}$=14 dB) is necessary to have a BEP less than 10^{-6}. This means that the signal power in the receiver, S_{min} (dB), must be such that $\gamma_{0\,dB}=S_{min}-N \geq 14$ dB. Finally, the sensitivity of the receiver must be at least $S_{min}=14+N=-90$ dB$\underline{\Delta}-60$ dBm.

The principle to enable and to disable the analog blocks is presented in Fig. 6(a). A control voltage, $V_{control}$ (V), selects between the enable and disable functions. Normally, this control voltage is null, whose consequence is to keep the transistors M_{1x} in the cut-off state. However, when the control voltage is toggled to 1.8 V, the transistors M_{1x} start to conduct and the current sources constituted by the transistors M_{2a} e M_4 are activated. The transistor M_4 behaves as a resistor and the transistors M_{2b} and M_{2c} (and further if more transistors M_2 are available) act as current sources. Thus, the transistors M_{2b}–M_{2c} start to inject currents in the branches *Bias* 1 and *Bias* 2. The same idea applies to transistors M_{5b}, M_{5c} (and further if more transistors M_5 were available), but in this case and after to be activated, the current sources constituted by the transistors M_{5a} e M_3 put the transistors M_{5b}, M_{5c} for working as current sinks (branches *Bias* 3 and *Bias* 4).

The activation procedure also applies to the digital circuits. Fig. 6(b) illustrates how this principle can be used to control the digital blocks, where the transistor M_3 was included in the inverter constituted by M_1 and M_2. Normally, the control voltage, $V_{control}$ (V), applied to the gate of the transistor M_3 is null and the transistor M_3 is in the cut-off state. In this situation the power consumption of the inverter is negligible.

The experimental tests made to the RF CMOS transceiver showed a total power consumption of 6.3 mW for the receiver (4 mW for the LNA, and 2.3 mW for the envelope detector and post-amplifier) and 11.2 mW for the transmitter. The transmitter delivers a maximum output power of 1.28 mW (very close to the specified 0 dBm) with a power consumption of 11.2 mW. When enabled, the power at the output of the PA can be selected from the following values: 0.22, 1.01 and 1.21 mW. For the LNA, an S_{21} of 19.2 dB, a noise figure (NF) of 3 dB, a 1 dB compression point (IP1) at −9 dBm and a third-order intercept point (IP3) at −5.4 dBm were observed. The LNA has also a stabilization factor of K=1.8 (this amplifier is unconditionally stable, $K>1$). Fig. 7 presents the most important analyzed results.

Table 1 lists the possibilities of transmitted power for any combination of the power selection signals and Fig. 8 shows a photograph of the first prototype of the RF CMOS transceiver, which occupies an area of 1.5 × 1.5 mm^2.

Tables 2 and 3 compare, respectively, the blocks of receiver and transmitter with those found in the state-of-the-art for similar applications and markets of the RF CMOS transceiver at 2.4 GHz.

The sensitivity of the Bluetooth receivers presented in [7,19] is very close. The power consumption observed in Darabi et al. [7] is higher than that observed in Hioe et al. [19], but this is not surprising because the process used in [19] is more power-saving when compared with the one used in [7]. The third-order intercept point (IP3) trades with the power supply voltage and with the power consumption [20]; thus, to have a higher IP3 in the first receiver is an obvious consequence.

The power consumption of the Global Positioning System (GPS) receiver presented by Gramegna et al. [21] is in a middle position, when compared with the other receivers listed in Table 2. The explanation for such behaviour is because this type of receivers must present very high sensitivities; thus, a compromise between the power consumption and the LNA's gain must be achieved or the sensitivity will not target the specification [20].

The low power consumption of the OOK/FSK (On–Off Keying/Frequency Shift Keying) receiver in Enz et al. [15] is achieved because the transistors operate in the moderated inversion mode. In fact, this RF chip can operate in the strong inversion with currents three orders of magnitude below the currents in saturation mode [15]. The main drawback to decrease drastically the power consumption is to operate with small RF frequencies as it is the case of the 433 and 861 MHz found in this RF CMOS transceiver.

In conclusion, the receiver of the RF CMOS transceiver at 2.4 GHz is the one that offers the best combination of all characteristics as a whole, e.g., power consumption, frequency of operation, selectivity, voltage supply, IP3 and sensitivity.

The CMOS process in the fabrication of the transmitter presented in Chee et al. [22] is the one that achieves the lowest power consumption. Moreover, the fact that it also operates in the lowest frequency (at 1.9 GHz) is another reason for consuming less power.

The modulation of the transmitters in Darabi et al. [7] and Choi et al. [10] is the main reason behind their high power consumptions. The transmitters presented in [7,10] were fabricated to operate, respectively, in Bluetooth and in IEEE LR–WPAN (IEEE) 802.15.4 networks with the Gaussian Frequency Shift Keying (GFSK) and the Gaussian Minimum Shift Keying (GMSK) modulations. Both Gaussian modulations use spread spectrum techniques to minimize the interference with the cost to increase the power consumption.

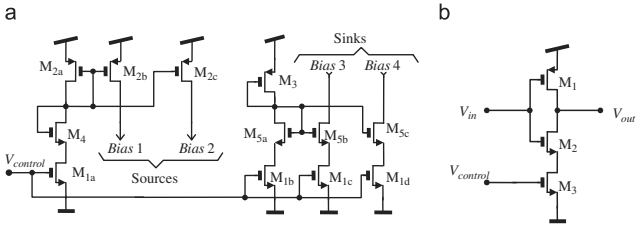

Fig. 6. The circuits (a) to enable and disable the analog blocks and (b) to enable and disable the digital blocks.

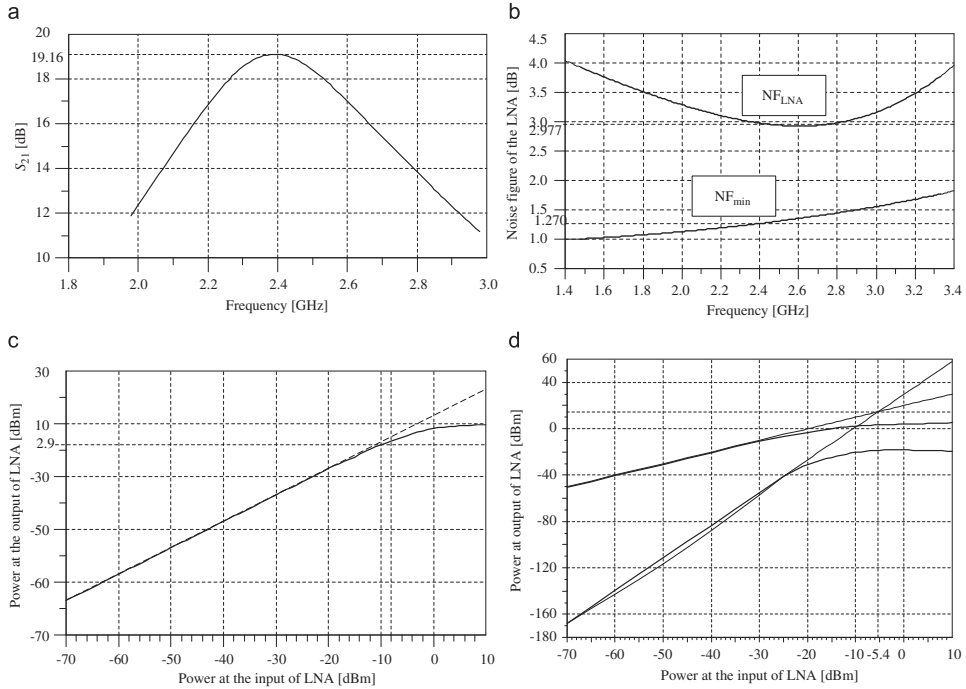

Fig. 7. For the LNA: (a) the S_{21} (dB) parameter, (b) the NF (dB), (c) the 1 dB compression point (IP1) and (d) the third-order intercept point (IP3).

Table 1
For the four combinations of the selection signals: the power consumption in the transmitter, power amplifier and respective transmitted power.

Power_select1 Power_select2 combinations	Power consumption of the transmitter (mW)	Power consumption of the Power amplifier (mW)	Transmitted power (mW)
0 0			
0 1	10.67	4.97	0.28
1 0	12.62	6.91	1.01
1 1	13.61	8.02	1.21

The transmitter presented by Charlon et al. [9] has two drawbacks. The first is the fabrication technology used. This transmitter was fabricated in a SiGe BiCMOS process, which per se presents high power consumptions; at the same time, it is supplied with a higher voltage of 2.8 V, compared to the previous ones of 1.2 and 1.8 V. Moreover, the multi-carrier modulation used in the IEEE 802.11b wireless networks requires high power consumptions.

Finally, as it happens with its receiver's block, the transmitter in Enz et al. [15] can use the ASK and FSK modulations with a voltage supply of 1.2 V. Internally, this transmitter was also designed to work in the inversion mode in order to support a minimum voltage of 0.9 V. However, this transmitter has a little high power consumption than was expected in the inversion modes, because the transmitted power is also high and a trade exists between the power consumption and the transmitted power.

Once again, the transmitter of the RF CMOS transceiver at 2.4 GHz presented in this work is the one that globally shows the best combination of characteristics, e.g., the radiated power, power consumption and frequency of operation.

3.4. Hot features concerning ESD protections

Integrated microdevices use bondingpads to connect the dies to external circuits and/or to PCBs. Normally, during the chip design it is necessary to prevent two possible effects: the first is the latch-up. The latch-up can change the behaviour of the circuit, as well as to destroy it [23]. The second effect is the electrostatic discharge (ESD), which can destroy the circuits on the die [24]. CMOS is, among all technologies, the most sensitive to ESD destruction. This takes place with the occurrence of the breakdown of dielectrics. Such a breakdown establishes a conductive

path in the silicon-oxide that separates the gates of MOSFETs from the channel. The resulting currents can be high and thus it can melt the surface of the die with the total destruction of the die. During the design and fabrication of the previous RF CMOS transceiver at 2.4 GHz, two levels of protections were considered [25]: the first level is to ensure protection of the input/output circuits (the circuits immediately connected to the bondingpads). The destruction resulted of discharges coming from one of the supply-rails is avoided with the second level of protection. This level is implemented by a power-clamp constituted by a transistor of N-type with the gate connected to the ground.

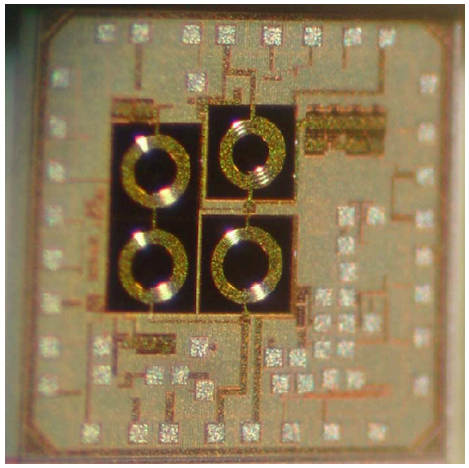

Fig. 8. A die photograph of the fabricated RF CMOS transceiver at 2.4 GHz.

The RF CMOS transceiver at 2.4 GHz shown in Fig. 9 has diodes anti-ESD with a total capacitance of 1.57 pF; thus, the input of the LNA no longer matches the antenna. This increases the return loss at the input, and for the same power transmission, it decreases the range. The decrease in the range due to the protection diodes was calculated to be from 10 to 5.5 m. A way to keep the range is to transmit the signals with a power of at least 3.3 mW, in order to compensate the unexpected 5.2 dB of losses. A perfect match between the antenna and the LNA can be achieved with external elements to overcome the undesired effects of the anti-ESD capacitance.

Two matching techniques can be used to improve the behaviour of the LNA. First, it can be used as a classical matching network with a series inductance, L_s = 1.5 nH, and a parallel capacitor, C_p = 3 pF. The second matching technique uses a series-stub with characteristic impedance of 40 Ω and electrical length of 30°, and an open-circuited parallel-stub with characteristic impedance of 55 Ω and electrical length of 69°. Fig. 9 shows four situations for the reflection coefficient, k_R, at the input of the LNA: (a) ideally without anti-ESD protections; (b) with anti-ESD protections but no compensation; (c) with a compensation (matching) network made of lumped elements and (d) with a compensation network made of transmission lines. In the two situations where the matching is achieved, the reflections decrease to acceptable values.

The additional protection level consists of a power-clamp. A power-clamp is made of a transistor of N-type with the gate and source connected to the ground and with the drain connected to the highest potential (1.8 V) supply-rail, V_{dd}. Normally, the nMOSFET transistor is in the cut-off state and when the power supply rises above an acceptable value, the transistor enters in the conduction state [26]. In this situation, the impedance between the supply-rails decreases to a low value when compared with the rest of the circuit in the microdevice. A set of power-clamps was designed for the RF CMOS transceiver at 2.4 GHz. Each class of circuits (the RF, digital and the analog circuits) inside the microdevice has its own power-clamp. A serial resistance limits the discharge current, in order to prevent the destruction of the microdevice. An implantation of a supplementary layer in the zone of drain makes the ESD protections more effective and more robust to discharge currents. The widths of the N-type transistors must be as high as possible to allow the discharge currents to flow better [27]. The power-clamp is a parallel of four N-type transistors with individual ratios, W/L, of 12.5/0.36 (μm/μm). The behaviour of the power-clamp was analyzed, when subjected to an ESD voltage of 4 kV. The measurements showed a maximum discharge current of 32 mA and a voltage between the drain and the source of the transistor below 35.4 V. These results revealed to be promising, since the dissipated power in the whole clamp was only 1.13 W. Moreover, transistors with ratios, W/L, of 12.5/0.36 (μm/μm) decrease the parasitic capacitance between the drain and the source compared to a large-width transistor and the consequence is less interference with the RF signal.

Table 2
Comparison of RF receivers found in the state-of-the art with the receiver's block of the RF CMOS transceiver at 2.4 GHz.

Receiver	Freq. (GHz)	Technology (μm)	Sensitivity (dBm)	IP3 (dBm)	Power consumption (mW)	Voltage (V)	Modulation/application
This work	2.4	0.18	−60	−6.4	6.3	1.8	OOK
Darabi et al. [7]	2.4	0.35	−82	−7	126.9	2.7	GFSK
Choi et al. [10]	2.4	0.18	−82		21	1.8	DSSS GMSK
Charlon et al. [9]	2.4	0.25	−77	+15	140	2.8	IEEE 802.11b
Hioe et al. [19]	2.4	0.18	−88	−15	65	1.8	GFSK
Gramegna et al. [21]	2.4	0.18	−130		30.6	1.8	GPS
Enz et al. [15]	433/862 (MHz)	0.18	−117 −111	−35/−32	2.5	1.2	OOK FSK

Table 3
Comparison of RF transmitters found in the state-of-the art with the transmitter's block of the RF CMOS transceiver at 2.4 GHz.

Transmitter	Freq. (GHz)	Technology	Radiated power (dBm)	Power consumption (mW)	Voltage (V)	Modulation/application
This work	2.4	0.18 μm	0	11.2	1.8	OOK
Chee et al. [22]	1.9	0.13 μm	0	1.8	1.2	OOK
Darabi et al. [7]	2.4	0.35 μm	4	124.2	2.7	GFSK
Choi et al. [10]	2.4	0.18 μm	>0	21	1.8	DSSS GMSK
Charlon et al. [9]	2.4	SiGe BiCMOS	−5	128.8	2.8	IEEE 802.11b
Enz et al. [15]	433/862 (MHz)	0.18 μm	10.5/9.5	36/39	1.2 1.2	OOK FSK

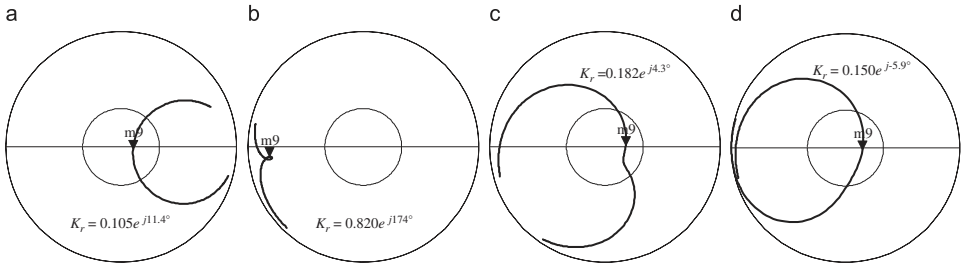

Fig. 9. Four situations of the reflection coefficient, k_R: (a) ideally without anti-ESD protections, (b) with anti-ESD protections, (c) with compensation network made of lumped elements and (d) with a compensation network made of transmission lines.

4. Applications of low-power RF microsystems

The interest in the development of low-power/low-voltage wireless microsystems is justified by the fact that energy scavengers are currently emerging for a number of applications from automotive to medicine. Microenergy scavengers are small electromechanical devices that harvest ambient energy and convert it into electricity. Energy scavengers could harvest different types of energies. Solar energy can be harvested with photovoltaic solar cells, thermal energy can be harvested with thermoelectric generators, mechanical energy can be harvested with piezoelectric, electromagnetic or electrostatic converters, and finally electromagnetic energy can be harvested through RF resonators. There exist two types of energy scavenging systems: macroenergy scavengers, typically in the cm^3 range, and microenergy scavengers, typically in the mm^3 range and manufactured using micromachining techniques. Microenergy scavengers are still in the R&D phase. Direct thermal-to-electric energy conversion without moving mechanical parts is attractive for a wide range of applications because it provides compact and distributed power, quiet operation, and is usually environmentally friendly. Thus, worldwide efforts are undertaken to expand the technology of thermoelectric devices into the field of microsystems technologies (MEMS). Previsions made by the specialists of the microsystems area show that the most expected growth of these devices will be with medical applications. An emerging technology for ultra-low-power communication platforms triggered renewed interest in power sources for wireless-sensor, in special wireless-wearable sensors, with power consumption nodes of few mega Watt. Today, almost all of these platforms are designed to run on batteries, which not only have a very limited lifetime but also, in many areas, are a cost-prohibitive solution. An attractive alternative is powering the sensors with energy harvested from the environment. Thus, interest is growing in solutions for energy microgeneration through energy harvesting by taking advantage of temperature differences. A viable energy source for low-powered devices such as microsensor systems, ZigBee chipsets, wearable electronics, implantable-medical devices, active-RFID tags and many other applications is possible, provided a temperature difference exists between the two surfaces of a thermoelectric microgenerator (in a wearable device, the difference between the body and the environment can be tens of degree, depending on the environment temperature). This temperature difference can be converted into electrical energy using the Seebeck principle [28]. Since many wireless sensors are powered in a peak basis (e.g., the transmission of data needs much more current than standby or receiving mode) and the temperature gradient could not always be present, the energy is stored in a rechargeable thin-film battery of the Li-ion type (integrated in the system). Ultra-low-power electronics performs DC–DC rectification with a variable conversion factor and recharge the battery on optimal conditions. Since a small volume is required, integration into an IC is desirable. A single-chip-regulated thermoelectric power source is the final goal to be achieved.

The fabrication of macroscale thermoelectric devices is based on the standard technologies for decades. Bismuth and antimony tellurides were used as thermoelectric materials since these materials have the highest performance figure-of-merit (ZT) at room temperature [29]. The co-deposition method was used to fabricate these thermoelectric thin films. A very stable evaporation rate of each element (Bi/Te and Sb/Te for the bismuth telluride and antimony telluride, respectively) allows the deposition of polycrystalline n-type and p-type materials, when the substrate is heated in the range 200–300 °C. The design of a thermoelectric microdevice with vertical microcolumns, connected in series by metal contact areas, requires the application of microsystem technologies. Reactive ion etching, lift-off and wet-etching (hydrochloridric acid/nitric acid solution) techniques were tested to create the vertical columns. A thin (50 nm) layer of nickel (deposited by e-beam) interfaces between the thermoelectric material and the metal contact areas (1 μm of aluminum) prevents the diffusion of the metal from the contacts into the thermoelectric film. The contact resistance plays a major role in the performance of the device, and a value smaller than 1×10^{-6} Ω cm^2 was achieved. A silicon substrate was used for integration with microelectronics, while at the same time providing good thermal contact with heat source and sink. The fabricated battery as well as all the electronic circuitry received the energy and recharged a thin-film integrated Li-ion battery (open-circuit voltages between 1.5 and 4.2 V, maximum current of few mA/cm^2 with a charge-storage capacity around the 100 μAh/cm^2).

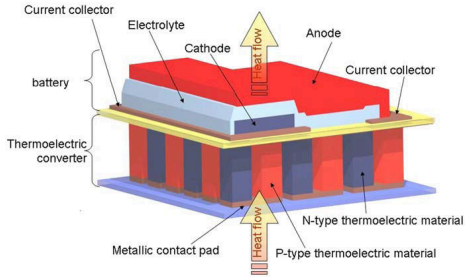

Fig. 10. A complete thermoelectric microsystem.

Fig. 10 shows an artwork of a complete thermoelectric microsystem with a thin-film solid-state battery placed on the top. When the heat flows across the junction, an electrical power current is generated by the Seebeck effect.

As the final goal of thermoelectric scavenging energy microsystems is to supply the wireless acquisition modules in wireless sensors networks, these must present low power consumptions in order to match with the power sources, as a way to put these same modules for working without human intervention, e.g., either to switch the battery or to recharge it.

5. Future trends

The future of RF microsystems needs the use of MEMS (Micro Electro Mechanical Systems)-based components [30]. An example of such a component can be the generator of the reference frequency used in the PLL. Crystal-based piezoelectric oscillators normally require a huge area, compared with those used by the associated electronics (when they exist, the inductances and capacitors are not included in this set); thus, an additional space must be provided in the PCB (Printed Circuit Board) with the inevitable consequence of an increase in the total production cost. Moreover, the accuracy and the stability of the produced frequency by these oscillators are temperature dependent and the error will be multiplied by the PLL, e.g., if the actual reference frequency is $f_{ref2}=f_{ref}(1\pm\Delta f)$, the actual carrier frequency will be

$$f_{out2}=Nf_{ref2}=Nf_{ref}\pm Nf_{ref}\,\Delta f=f_{out}\pm\Delta f_{out} \quad (2)$$

where N is the division ratio of a PLL, f_{ref} (Hz) the error-free reference frequency of a PLL, $\pm\Delta f$ (Hz) the drift (above or below) in the reference frequency, and f_{out} (Hz) the error-free carrier frequency. A special issue must be taken into account, specially for high division ratios, N, and high reference frequencies, f_{ref} (Hz), in the PLL, because the overall drift (or propagated error) in the frequency at the output of the PLL, $\Delta f_{out}=Nf_{ref}\cdot\Delta f$ (Hz), can be critical. Beyond the advantage of having small area occupancy, MEMS resonators allow one to obtain an accurate trimming in the frequency of oscillation. Moreover, as this adjustment could be made in an electrical form, it constitutes a remarkable advantage over the crystal oscillators [31].

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