ESD protection on RF transceivers: impact and improvement strategies

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ABSTRACT

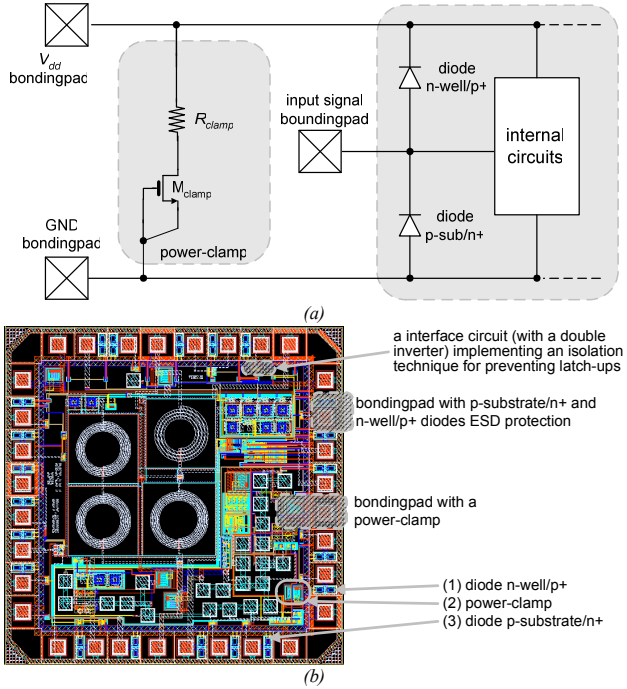
The discharges resulted from static electricity is the major cause of integrated circuits fail and destruction. The electrostatic discharge (ESD) protections are the only effective way to protect the internal circuits in the microdevice. This also applies to RF integrated circuits but with the cost to change its behaviour relatively to their specifications. One focus of this chapter is the identification and quantization of how these ESD protections contributes for deviating from the targeted specifications. The parallel capacitance and the serial resistance of ESD protections have a strong effect in the behavior of RF transceivers when working at high frequencies. The usual methodology for design RF transceivers is following an integrated form and including the ESD protections. The ESD protections have direct impacts in the power amplifier's design because the transmission range must be the initially specified one. This chapter also presents two compensation strategies for RF transceivers designed without including the ESD protections, which were included later and independently. All experiments and simulations were carried out with a 2.4 GHz RF CMOS transceiver fabricated in the UMC 0.18 µm RF CMOS process.

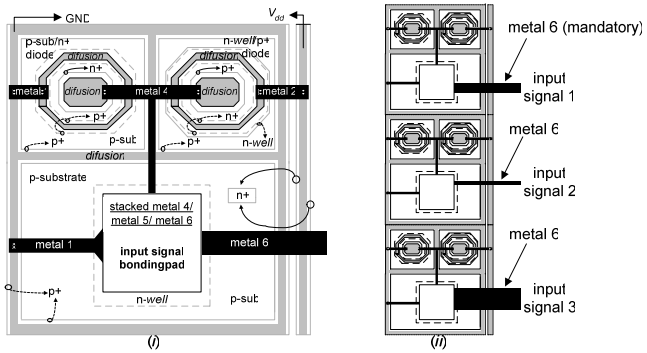
1. INTRODUCTION

The electrostatic discharges (ESD) destruction is an issue of high focus when designing electronic circuits in CMOS technologies. An electrostatic discharge can result in the breakdown of dielectric oxides (for isolating the gates and channels of MOSFETs), whose consequences are the establishment of currents with potential for destroying the circuits of the whole microdevice (Ker *et al*, 2002). These currents are produced at exterior of the microdevice and flow to its interior across the bondingpads (bondingpads are fundamental elements used for connecting the microdevice to external circuits and/or PCBs). The intensity of the ESD currents can be high enough to make the surface of the microdevice melting with the consequent destruction.

The CMOS technology allows the fabrication of non-floating p-substrate/n+ and n-well/p+ diodes. In this sequence, the Figure 1(a) illustrates the two most usual protection levels against ESD currents (Ker *et al* 2005, Ker *et al* 1999). In the first configuration, a p-substrate/n+ and a n-well/p+ diodes connects respectively, an input signal bondingpad (used for injection of input signals into the internal circuits of the microdevice) to the ground (the smallest potential) and to the V_{dd} (the highest potential) rails. Normally, the ESD currents are steered by one of the diodes for ESD voltages (which can either be positive or negative) above their threshold voltages. The second configuration prevents the occurrence of ESD discharges (originated from one of the supply-rails) into the internal circuits. This level of protection can be achieved with power-clamps, which are not more than N-MOSFETs with their gates connected to

the ground (Ohletz *et al* 2009, Ker *et al* 2003a, Ker *et al* 2006, Wang *et al* 2001, Koo *et al* 2009). Contrary to p-substrate/n+ and a n-well/p+ diodes, the power-clamps are not fully discussed in this chapter because their effect in the RF performance of microdevices is negligible (e.g., the points subjected to the RF signals are not directly connected to none of their terminals). The Figure 1(b) shows the chip layout of the RF transceiver used as case study in this chapter, where it can be observed bondingpads with ESD protections based on non-floating p-substrate/n+ and n-well/p+ diodes, as well as bondingpads protected by power-clamps (placed between the supply rails). The schematic in the Figure 1(c) refers to a ESD protected bondingpad for providing input signals to the internal circuits. The schematic in the projection (*i*) illustrates the supply rails that surround the whole chip, as well as the layout masks used for their implementation. The projection (*ii*) of the Figure 1(c) illustrates the modularity concept for connecting each boundingpad (this projection uses three bondingpads with input signals).





(c)

Figure 1: (a) The most common configurations for protecting against ESD discharge, when doing a design of a RF chip. (b) Chip layout and respective protections of the RF transceiver used as case study. (c) Schematic showing the construction details of a bondingpad for input signals protected by n-well/p+ and p-substrate/n+ diodes and connection with three bondingpads with ESD protections.

Another undesirable effect are the injection of high currents into microdevices due to electrostatic discharges (ESD) whose major effect can be the destruction of these same microdevices (Feng *et al* 2004, Bafleur *et al* 1995, Chebli *et al* 2010, Ker *et al* 2005, Choi *et al* 2005). The state-of-art showed that the ESD induced parasitics have been tolerated by regular ICs and hence, have been largely ignored by IC designers. However, these parasitics are becoming real limiting factors in radio-frequency (RF) and high-speed applications (Vinson *et al* 1998, Wang *et al* 2005, Ker *et al* 2011).

Finally, it must be noted for information purposes that the latch-up effect constitutes another interface phenomena potentially dangerous for submicron CMOS technologies. The restriction posed by this effect is illustrated in the Figure 2(a), showing a lateral projection of a CMOS inverter with a parasitical p-n-p-n structure (Ker *et al* 2003b). For illustration convenience, this figure don't show neither the gates of MOSFETs nor the outputs. This parasitical structure can originate a latch-up situation. As showed in the Figure 2(b), a conduction path is established through the vertical pnp bipolar transistor (Q_{pnp}) and then through the coupled lateral npn bipolar transistor (Q_{npn}). An effective way to prevent such a problem in the circuits directly connected to the bondingpads is surrounding them with two active regions with opposite polarities (UMC 2005a). As showed in the Figure 2(c), the NMOS transistors are surrounded by an external ring (designated as diffusion ring) doped with a p+ material (boron) that connects to the V_{dd} power-rail. There is also available an inner ring, whose diffusion zone is doped with a n+ material (phosphorus) and connects to the ground. This second ring isolates the active regions, where the channels of the two MOSFETs (NMOS and PMOS) are located. The implantation of a n-well region around this second ring (and around the first ring, for the case of a PMOS transistor) provides an increased isolation between the two MOSFETs because a n-well implantation is deeper than the n+ and p+ implantations. This results in a more effective barrier to the latch-up currents (Ker *et al* 2003b). Moreover, the UMC foundry himself recommend that the internal circuits (that are not directly connected to the boundingpads) must present a minimum distance from the interface circuits (the circuits directly connected to the boundingpads) (UMC 2005a).

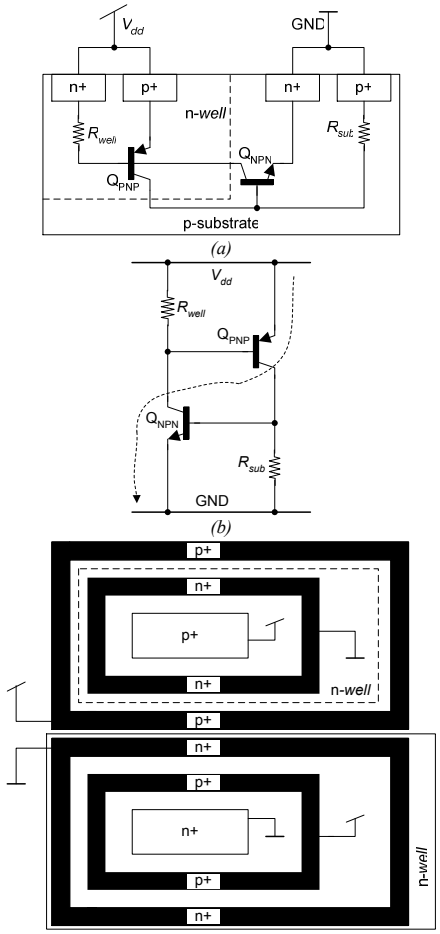


Figure 2: (a) Lateral projection of a CMOS inverter; (b) equivalent circuit due to the latch-up phenomena (Ker et al 2003b); and (c) used isolation technique for preventing latch-ups.

A 2.4 GHz RF CMOS transceiver was used a case study for better illustration the contributions of this chapter. In this sequence of ideas, the first set of contributions presented in this chapter includes the mechanism identification of how ESD protections can produce deviations from the initial specifications,

as well as how to measure these same deviations. The second set of contributions is the proposition of two compensation strategies for applying on RF transceivers designed without the inclusion of ESD protections and which were further included. To finish, it must be noted that the RF transceiver under analysis was designed and fabricated in the UMC 0.18 μm RF CMOS process. The RF CMOS transceiver was designed to met the following specifications: a receiving sensibility of –60 dBm with a power consumption of 6.3 mW and a maximum transmitting power of 0 dBm (1 mW) with a power consumption of 11.2 mW for obtaining a range of ten meters. The Figure 3 illustrates some bottlenecks associated to the ESD protections (e.g., parasitic capacitances and resistances) that must be take in account and fixed for keep the former specifications.

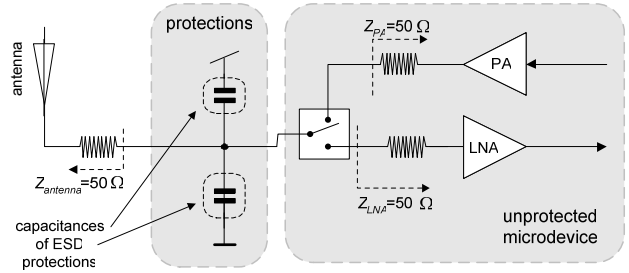
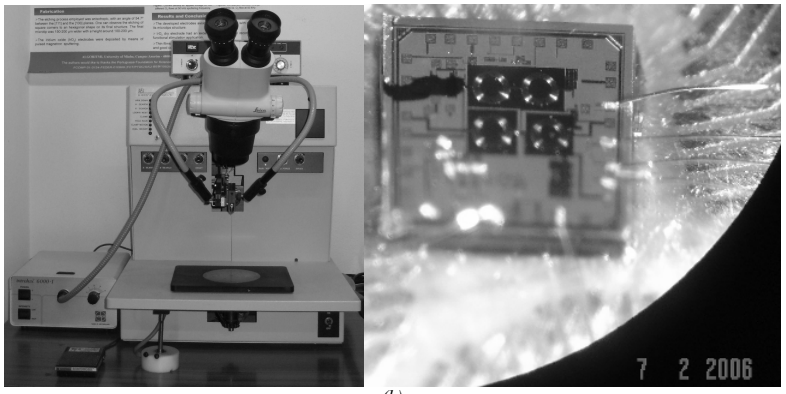


Figure 3: The possible effects that can result with the presence of ESD protections.

2. EXPERIMENTAL

A probe station (model Karl Suss AP4) and a wirebonding machine (model MEI 1204W) were used for doing the measurements applied to the RF transceiver at 2.4 GHz. The photographs in the Figures 4(a) and (b) are magnified views of the RF transceiver's microdevice to show the connections between the bondingpads and an external PCB. The wire connections illustrated in the Figure 4(b) were made done by aluminium with a diameter of 20 μm.

(a)



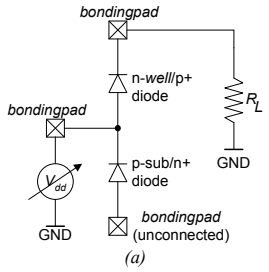
(b)

Figure 4: Photographs with a magnified view of the die used (a) within the setup based on a probe-station and (b) within the setup based on the wirebond machine.

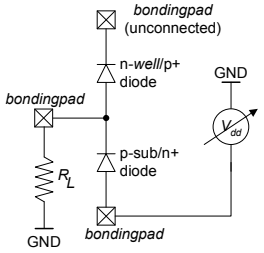
A DC voltage was applied at the input of the LNA and swept for measuring the currents and the voltages across the diodes used for doing ESD protection, e.g., the p-substrate/n+ and n-well/p+ diodes illustrated in the Figure 3. The Figure 5 shows the used setup, while the Figure 5(b) shows the obtained results. In this sequence, it can be observed the serial resistance (R_d) and the threshold voltage (V_{th}) of these diodes in the Table I, whose values were obtained after doing the linear fit of the measured current/voltage (I/V) characteristics.

Table I:The serial resistance, R_d, and the threshold conducting voltage, V_{th}, of the ESD protection diodes.

	p-substrate/n+ diodes	*n*-well/p+ diodes
R_d (Ω)	25.9	25.9
V_{th} (mV)	767.2	767.2



(a)



(b)

Figure 5: Used setup for obtaining the I/V characteristics of the (a) n-well/p+ and (b) p-substrate/n+.

The precise knowledge of parasitic capacitances of the ESD protections is of major interest because they have a strong effect in the behavior of RF transceivers at high frequencies. Therefore, the quantization of these capacitances is important for predicting the behaviour of the microdevice, in order to implement compensation techniques to minimize their impacts. The capacitance of a generic pn junction is given by (Baker 2010):

$$C = \frac{C_j A_d}{(1+\frac{V_d}{\phi_0})^{m_j}} + \frac{C_{jsw} P_d}{(1+\frac{V_d}{\phi_0})^{m_{jsw}}} \; [F] \qquad (1)$$

where V_d [V] is the DC reverse voltage bias, ϕ_0 [V] is the potential value of the junction, and A_d [m^2] and P_d [m], are the area and the perimeter of the ESD protection diodes. The SPICE parameters of the CMOS process for fabricating the RF CMOS transceiver at 2.4 GHz used as case study are as follows (UMC 2002b): C_j=0.00119 F.m^{-2}, C_{jsw}=1.6×10^{-10} F.m^{-1}, ϕ_0=0.79 V, m_j=0.515, m_{jsw}=0.381 for the P-substrate/N+ diodes, and C_j=0.00114 F.m^{-2}, C_{jsw}=1.74×10^{-10} F.m^{-1}, ϕ_0=0.762 V, m_j=0.395, m_{jsw}=0.324 for the N-well/P+ diodes. The worse value of the ESD capacitance was selected from the set of values obtained after sweeping the voltage V_d. The highest capacitance (corresponding to the worse value) of C≈1.57 pF was obtained by doing the capacitances summation of the p-substrate/n+ diode and n-well/p+ diodes ($C_{nwell/pP+}$ and $C_{psub/n+}$, respectively). This parallel capacitor makes the Low-Noise Amplifier (LNA) to be unmatched when connected to an antenna with impedance of 50 Ω. This increases the return loss at the input of the LNA and decreases the signal transmission from the antenna to the LNA. In this situation and keeping the transmitting power unchanged, the distance between the transmitter and the receiver (e.g., the range) must decrease in order to provide signal with same power at the input of the LNA (as well as, at the output of the LNA and on further stages of the receiver). If nothing is done in terms of power amplifier design, the range decreases from 10 meters to approximately 5.5 meters (almost to the half of the nominal value) after including the previous capacitance. The alternative solution is increasing the transmitted power from 1 mW to about 3.3 mW. Another solution for keeping the range equal to 10 m is increasing the power of RF signals at the output of the power amplifier (PA) from 1 mW to about 3.3 mW. This last solution can compensate the return loss of 5.2 dB in the LNA input. However, this last solution is not acceptable because it requires a transmitter with an higher power consumption, whose consequence is a reduction in the useful life of batteries. Under these conditions, the acceptable solution is giving mechanisms to provide a perfect match between the antenna

and LNA. The matching condition in the LNA can be achieved with the help of external elements, which can be either lumped or distributed.

3. SIMULATION RESULTS

3.1 Receiver (Low-Noise Amplifier, LNA)

The Figure 6 shows two solutions to improve the behavior of the circuit. The first network is constituted by a classical matching network, which is composed by a series inductance (of L_s=1.5nH) and a parallel capacitor (of C_p=3pF). The second solution uses a series-stub (with a characteristic impedance of 40 Ω and an electrical length of 30º) and an open-circuited parallel-stub (with a characteristic impedance of 55 Ω and an electrical length of 69º). The inductance of wirebondings made of aluminium was taken in account in the two previous solutions. These additional inductances have been calculated to be 0.9 nH/mm (Alimenti 2003).

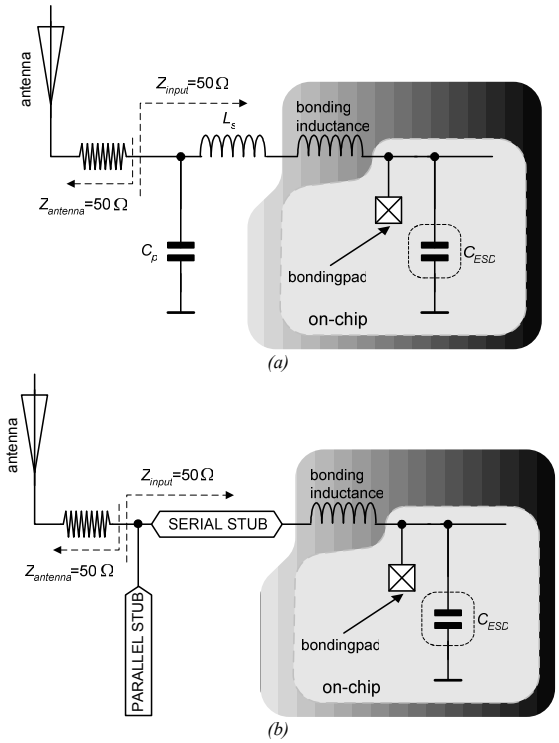
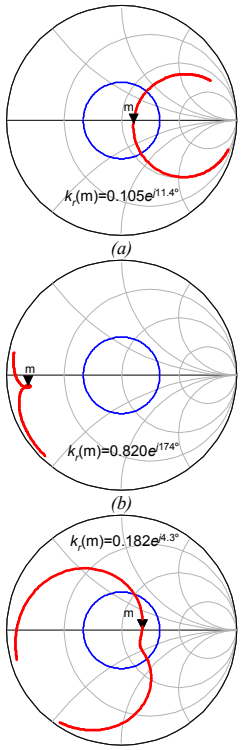


Figure 6: Matching networks for compensating the effects that arise due to the capacitances of the ESD protections for the following implementations: (a)with lumped circuit-elements, and (b)with transmission lines.

The Figure 7 shows the simulation results of four situations for the reflection coefficient, k_R, in the interface between the antenna and the input of the LNA: (a) the ideal behavior without the effect of the ESD protections; (b) the unmatched behavior due to the effect of the ESD protections; (c) the matched behavior after doing the compensation (matching) with a network made of lumped elements, and (d) the matched behavior after doing the compensation (matching) with a network made of transmission lines. It can be observed that the reflection decreased to acceptable values after doing the matching procedures. Also, the reflections decreased to acceptable values with the reflection coefficient, k_R, being steered to very close the center of the Smith's chart. The use of transmission lines is more suitable than using lumped elements because the lithography processes allows their fabrication with high reproducibility. Moreover, laser trimming techniques can also be used when a fine tuning of transmission lines is required.



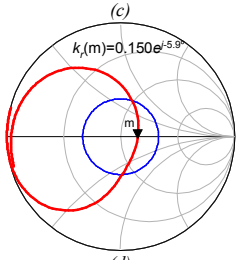


Figure 7: Simulations showing the reflection coefficient, k_R, at the input of the LNA obtained: (a) for an ideal situation without considering the effect of ESD protections; (b) for the unmatched situation, considering the effect of ESD protections; (c) for a matched situation, considering a compensation network made of lumped elements, and (d) for a matched situation with a compensation network, implemented by transmission lines.

As illustrated in the Figure 8, the simulated group delay presents a quasi-flat behavior around the frequency of interest (e.g., the 2.4 GHz) for the matching situation achieved with lumped components. The use of matching elements made of transmission lines also resulted in acceptable values of the group delay. It was observed in this second matching situation a total bandwidth of 0.2 GHz (100 MHz for each side around 2.4 GHz). The results obtained with lumped elements promise good potential for broad-band applications. The $|S_{21}|$ [dB] of the LNA can also be improved with the both matching networks. From the $|S_{21}|$ point of view and without taking in account the fabrication specificities, there are no restrictions for using any matching technique (see the Figure 9). Finally, the simulated noise figure, NF [dB], of the LNA is illustrated in the Figure 10, where it can be observed that the worse (but still acceptable) situation happens when the lumped elements are used as matching networks. In this case, the value of the NF is located around 4 dB, whereas the transmission lines makes the NF to be lower than (but very close) 3 dB.

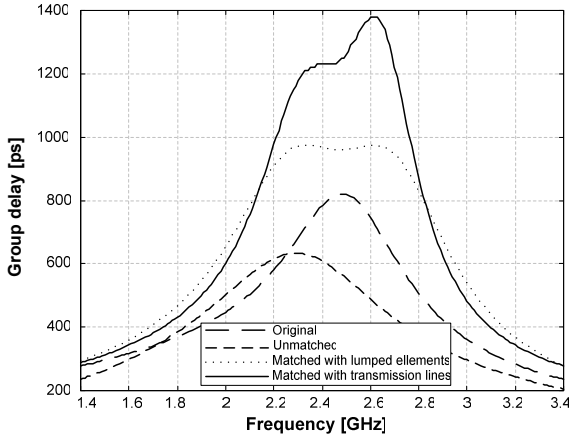


Figure 8: Simulations showing the group delay.

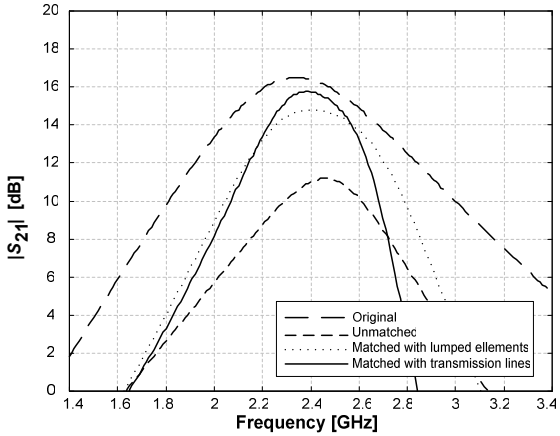


Figure 9: Simulated $|S_{21}|$ [dB] of the LNA.

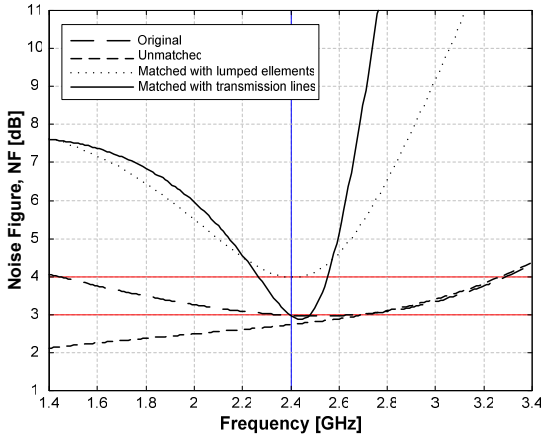


Figure 10: Simulated NF [dB] of the LNA.

3.2 Transmitter (power amplifier, PA)

Any transmitter contains a power amplifier (PA) to provide RF signals with an appropriated output power. The transmitter subsystem of the RF CMOS transceiver at 2.4 GHz of this chapter contains a cascade of five inverters in order to drive a ASK signal from the modulator circuit to the input of PA. As illustrated in the Figure 11, it is possible to select between to keep the transmitter off and to select between three different output powers. The transmitter uses two sets of *LC* networks for adapting the PA to the antenna. The L_1-C_1 elements of the first network reduce the second harmonic of the carrier, while the second network is tuned to the carrier frequency by the two L_2-C_2 elements.

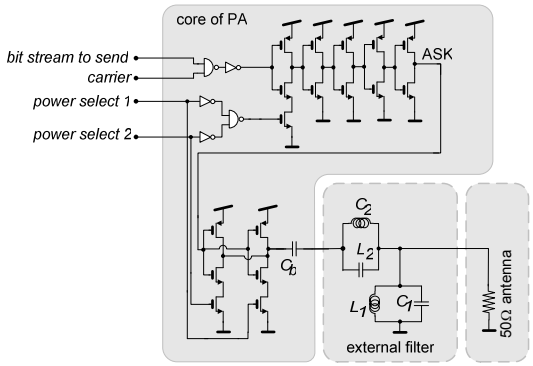


Figure 11: The schematic of the transmitter.

As it happened with the LNA for the case of receiver, the ESD capacitances also changes the matching conditions of power amplifiers (PAs). As demonstrated by the simulations, the previous parasitic capacitance of 1.57 pF makes the maximum power delivered to the antenna to fall from the nominal value to about 0.44 mW. In this situation, it is expected a decrease in the range to about 5.85 meters. The two solutions previously presented in the Figure 5 for the case of LNA can also be used to improve the behavior of the transmitter. The first network is constituted by a matching network composed by a series inductance (of L_s=5nH) and a parallel capacitor (of C_p=0.5pF). The second matching network is composed by a series-stub (with a characteristic impedance of 75.6 Ω and an electrical length of 40º) followed by an open-circuited parallel-stub (with a characteristic impedance of 83 Ω and an electrical length of 29º).

The Figure 12 shows the simulated reflection coefficient, k_R, in the interface between the PA and the antenna for these four situations: (a) ideally, without the effect of the ESD protections; (b) the unmatched case considering the effect of the ESD protections; (c) the matched case where a compensation network formed by lumped elements is used, and (d) the other matched case with the compensation network being formed by transmission lines. The degradation of k_R (dangerously near the unity) is evident in the situation (a), when nothing is done to compensate the ESD capacitance and justifies why the power transmitted into the antenna is only 0.44 mW. The methods based on lumped circuits and transmission lines resulted in powers at the antenna of 1.44 mW and 1.49 mW, respectively. This increase of powers at the antenna isn't strange because the $|k_R|$ decreases and is steered closed to the center of Smith Chart ($|S_{21}|$ increase as well as the power transmission from the PA to the antenna) after implementing one of the two matching technique, when compared with the ideal situation – see the Figures 11(a), (b) and (c).

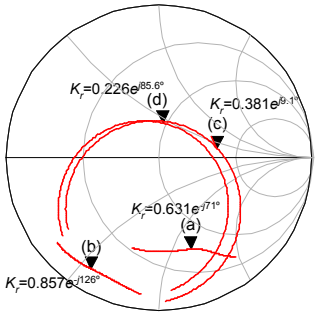


Figure 12: Simulations showing the reflection coefficient, k_R, at the output of the power amplifier obtained (a) ideally without considering the effect of the ESD protections; (b) for the unmatched situation considering the effect of the ESD protections; (c) for a matched situation considering a compensation network made of lumped elements, and (d) for a matched situation with a compensation network made with transmission lines.. All the k_R's include the effects of the blocking capacitor C_b and the LC external filter.

The Figure 13 shows the S_{21} parameter measured from the output of PA to the input of antenna (S_{21}) for the same situations illustrated in the Figure 11. These last parameters allows to know the available power of the PA that was really transmitted through the air. The degradation of k_R (dangerously near the unity) is evident on the situation (a) when nothing is done to compensate the ESD capacitance. Also, the wave transmission from the PA to the antenna is week in this situation and thus the transmitted power is also low - this justify why the transmitted power is only 0.44 mW. The methods based on lumped circuits and

transmission lines resulted in transmission powers of 1.44 mW and 1.49 mW, respectively. The increase observed in the transmitted powers are not strange, because when looking to the Figure 12 and comparing the two matching situations (c) and (d) with the situation (a), the improvement (when compared to the ideal situation) of the S_{21} parameter is evident. Thus, the comparison of the two matching situations (c) and (d) with the situation (a) allow to conclude that the wave transmission from the PA to the antenna was improved. Moreover, the Figure 13 confirms smaller reflections for the situations (c) and (d), whose points are closer the center of Smith Chart relatively to the situation (a).

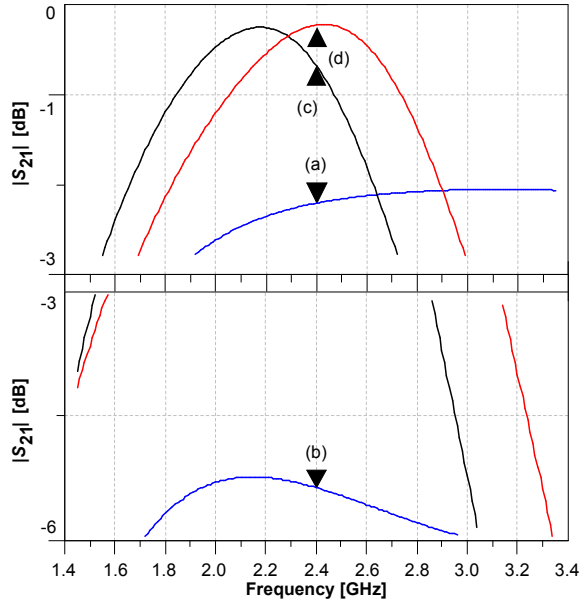


Figure 13: The S parameter measured from the output of PA to the input of antenna obtained (a) ideally, without the effect of the ESD protections; (b) with the effect of the ESD protections; (c) with compensation network formed by lumped elements; and (d) with a compensation network formed by transmission lines.

3.3 Power-clamp

A power-clamp is a n-type MOSFET with both the gate and source connected to the ground and with the drain connected to the supply-rail with the highest potential, V_{dd}, making this transistor to be normally in the cut-off state (Ker *et al* 2003a). If the power-supply rises above an acceptable value then, the impedance between the supply-rails across the channel of the MOSFET will decrease and the MOSFET. This impedance will be smaller than those observed in other circuit paths inside the microdevice, thus the ESD current is steered from these circuits and their destruction is then avoided. The power-clamps of the RF CMOS transceiver contains a serial resistance to limit the discharge currents, in order to prevent the

destruction of the microdevice by the power-clamp. The implantation of a supplementary layer in the drain's region make the ESD protections more effective and themselves more robust to discharge currents (Ker *et al* 2003a, Ker *et al* 2005, UMC 2005). The widths of the MOSFETs must be as high as possible, in order to have a better flow of the discharge currents (Ker *et a*l 2003a, UMC 2005). This power-clamp is a parallel of four (#4) MOSFETs with individual size-ratios of W/L = 12.5/0.36 [μm/μm]. The behavior of the power-clamp was analysed when this one was subjected to a ESD voltage of 4 kV. The results revealed to be promising because it was obtained a maximum discharge current of 32 mA and a voltage between the drain and the source of the transistor below 35.4 V, which corresponded to a dissipated power of only 1.13 W in the whole power-clamp. Moreover, the drain-source capacitance of four MOSFETs with individual ratios of W/L = 12.5/0.36 [μm/μm] is smaller when compared with that obtained with a single MOSFET with a ratio of W/L = 50/0.36 [μm/μm]. In this case, the interferences with the radio-frequency signals is smaller.

4. CONCLUSIONS

The parasitic capacitances of ESD protections can affect the behavior of an entire RF transceiver for high frequencies, especially the blocks of Low-Noise Amplifiers (LNAs) and Power Amplifiers (PAs). Moreover, an effective protection of the whole RF transceiver can only be achieved with ESD protection in the input/output pins. These two factors (e.g., the parasitics versus the level of ESD protection) trades between then and imposes severe problems. This is especially true in the case of power amplifiers (PAs) because a certain degree of mismatching can produce reflected signals with the consequence to have a smaller RF power transmitted into the antenna. However, in certain situations the reflected power can be significant and susceptible to destroy the PA (and the entire microdevice). The main contributions of this chpater was: (1) the identification of the main problems associated to the ESD protections (using a RF CMOS transceiver at 2.4 GHz as a case study to better illustrate the concept); and (2) the presentation of two compensation techniques for reducing the impacts of ESD protections. These techniques be implemented either with lumped elements or with transmission lines.

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