#### Micro and nanodevices for thermoelectric converters

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## **1** Introduction

The thermoelectricity consists in the conversion of temperature differences on electric energy and the contrary. Three effects are present in the thermoelectricity: the Seebeck effect, the Peltier effect and the Thomson effect. Thomas Seebeck (1770-1831) observed the arise of a voltage,  $\Delta V$  [V], after subjecting the junction of two different materials to a temperature gradient,  $\Delta T$  [K], and an electric current flowing in a load [1]. This effect can be quantified by way of the Seebeck coefficient,  $\alpha$  [ $\mu$ VK<sup>-1</sup>]:

 $\alpha = \Delta V / \Delta T$ 

(1)

The Seebeck effect can be used in two type of applications: for temperature sensors and thermoelectric generators [1]. The Figure 1 shows the two latter examples, where  $T_h$  [K] and  $T_c$  [K] (> $T_h$ ) are the temperatures in the hottest and in the coolest sides, respectively. In these examples, the temperature gradient  $\Delta T$  is equal to  $T_h$ - $T_c$  (and it is always equal for temperatures either in K or in °C).



## Figure 1: Seebeck effect, used as temperature sensor (a) or energy generator (b).

Jean Peltier (1785-1845) observed in 1834 that the flow of an electric current through the junction of two different materials had the consequence to release (heating) or to absorb (cooling) thermal energy. The Figure 2 illustrates these two examples, where the temperature in the junction rises or decreases, respectively [1]. Moreover, he observed that the released or the absorbed energy was proportional to the electric current. This effect is quantified by the Peltier coefficient,  $\pi$ . Some years later, William Thomson (later known as Lord Kelvin) established the relation between the Peltier and Seebeck coefficients:

(2)

where T[K] is the room temperatures.

 $\pi = \alpha T$ 



# 1.1 Macrodevices

In the sixties (60s), the thermoelectric phenomena was of major concern by researchers, when it was generally accepted that one of those days, the Peltier elements would be used in all cooling applications. However, in the four past decades, there wasn't a significant progress in this area. This was mainly due to the coefficient of performance (COP) of the Peltier elements being four to five times below to those found in conventional coolers (based on the Carnot cycle). Additionally, the unitary limit of the figure-of-merit,  $Z[K^{-1}]$ , (a performance measure of thermoelectric

materials) it was seemed as an impossible barrier to pass, but also unexplainable. The chalcogenide compounds, the bismuth telluride  $(Bi_2Te_3)$  and the antimony telluride  $(Sb_2Te_3)$  were known for decades as the best thermoelectric materials at room temperature. The figure-of-merit of a material is calculated by the following equation:

$$Z = \frac{\alpha^2}{\rho \kappa}$$

where  $\alpha$  [ $\mu$ VK<sup>-1</sup>] is the Seebeck coefficient,  $\rho$  [ $\Omega$ m] is the electric resistivity and  $\kappa$  [Wm<sup>-1</sup>K<sup>-1</sup>] is the thermal conductivity. The figure-of-merit can also be calculated for a specific room temperature, *T* [K], and it results in the following dimensional quantity:

(3)

$$ZT = \frac{\alpha^2}{\rho\kappa}T$$
(4)

In spite of its inferior performance, the cooling applications based on Peltier devices don't require maintenance because there are no movable parts. The Figure 3 shows a conventional Peltier module, constituted by thermoelectric elements between the two ceramic foils. The ceramic foils must be good thermal conductors to minimize their effect on the performance of the Peltier device. The smallest device (between the wires) is a miniaturized Peltier module made with thermoelectric micropairs is also depicted.



Figure 3: A photograph showing conventional and miniaturized Peltier modules.

# **1.2 Microdevices**

The use of thin-films deposition techniques with microsystems technologies renewed interest in the thermoelectricity. Integration of efficient solid-state thermoelectric microdevices with microelectronics is desirable for local cooling and thermoelectric microgeneration, since they can be used to stabilise the temperature of devices, decrease noise levels and increase operation speed. An array of such devices can also be used for lab-on-chip applications, where the precise temperature control is required. Despite the range of exciting applications, only few approaches to manufacture thermoelectric devices with small dimensions were reported up to now [3-6]. Also, the Peltier devices can convert thermal energy to electrical energy, because they are reversible. Electronic devices with low-power consumptions can be supplied with these energy converters. Examples of electronic devices include electronics embedded in wearables, wristwatches, among others. The last application has been widely explored by Seiko [7] and by Citizen [8]. The Citizen's Eco-Drive Thermo watch contains a generator composed by 1242 thermoelectric elements capable to produce a voltage of 640 mV with a power of 13.8 µW, for each degree temperature difference. The Seiko's Thermic watch can generates 200 mV of voltage with 1040 Peltier elements under the same conditions.

Micropelt was the first company to deploy ready-to-use microcoolers in the market. This company was created under a joint-venture formed by the Infinion Technologies and the Fraunhofer Institute for Physical Measurement Techniques (IPM), and it presents a fabrication process that allows the fabrication of thermoelectric elements with reduced dimensions. This fabrication process uses two wafers (with the n-type and p-type elements) that are glued together in order to construct sub-millimetre sized Peltier elements. These Peltier present cooling capabilities above 100 Wcm<sup>-2</sup> [9] for gradient temperatures up to 30 K at the room temperature.

Efforts to use MEMS (Micro-Electro-Mechanical Systems) techniques in the fabrication of thermoelectric devices had been made by the Jet Propulsion Laboratory (JPL, NASA) and by IPM. An electrodeposition process is used by JPL [5], while at the same time a sputtering and dry-etching processes were developed by IPM to fabricate thermoelectric structures. Additionally, Völklein [10] explores the use of tellurides for fabricating thermoelectric sensors. Mr. Völklein also developed a technique to measure the thermal conductivity on thin-films.

Concerning the use of patterning techniques on thermoelectric films, few approaches were reported in the literature. Da Silva *et al* [11] uses lift-off with SU-8 photoresist to create vertical columns of thermoelectric materials. But due to the maximum working temperature of SU-8 photoresist, the thermoelectric properties of the thin-films incorporated in the devices are worse than those obtained in bulk materials, since 200-300 °C of substrate temperature is required to fabricate high-quality thermoelectric thin-films. Böttner *et al* [3] uses dry etching to pattern thermoelectric devices. Shafai [12] reported the patterning of thin-films by wet etching but no details were given about the process.

Doctor Wijngaards [13] fabricated Peltier microdevices in membranes by way of a process compatible with CMOS fabrication processes. However, the thermoelectric properties of the polycrystalline silicon material used in his work created temperature differences of only 2 K. Schavaevitz [14] presented at the Massachusetts Institute of Technology (MIT), a MEMS device to generate electricity from a thermal combustion microcamera. Such a device is based on a silicon-germanium thermoelectric converter. In this case, an electrical power of 450 mW was obtained from a temperature of 650 °C inside the combustion camera.

The ThermoLife® Energy Corp. (USA, Californa) imported technology from the former D.T.S. (Germany) to fabricate thermoelectric microgenerators [15]. This company reported the ability to produce 30  $\mu W$  - corresponding to 3 V, 10  $\mu A$  - from temperature gradients of 5 K in an area less than 1 cm². Stordeur and Stark were one of the first to fabricate thermoelectric microgenerators in flexible membranes [16].

New developments also took place at TU-Dresden in order to use flexible membranes to fabricate thermoelectric devices to provide autonomous energy sources for application in microsystems [17]. In this case, the electrodeposition and photolithography techniques were employed for fabricating the thermoelectric devices with thin-films of n- and p-types. However, these devices have the drawback to produce voltages of only 250 mV with temperature differences of 30 K.

To finish, it must be told that the works developed by Gao Min [18], Völklein [19] and Jacquot [20] are important contributions in the modelling field, and these models of cooling microdevices still are references in the thermoelectric area.

#### 1.3 Nanodevices and superlattices

Bismuth and antimony tellurides are the materials with the best known thermoelectric performances. However, the silicon process compatibility of polycrystalline silicon

germanium alloys makes them good thermoelectric material candidates. Devices, based on bismuth (Bi), antimony (Sb) and tellurium (Te) can support up to 250 °C. For higher temperatures, Silicon-Germanium (Si-Ge) compounds can be used, despite having poorer thermoelectric properties.

In today's best commercial thermoelectric modules (made of Bi, Sb and Te compounds), the figure-of-merit, ZT, is about 1, despite many attempts to find compounds with higher performance. In conventional tridimensional crystalline systems, the quantities S,  $\sigma$  and  $\kappa$  are interrelated and are difficult if not impossible to control them independently to improve the ZT [21,22]. An increase of S, usually results in a decrease of  $\sigma$ . A decrease of  $\sigma$  leads to a decrease of the electronic contribution to  $\kappa$ . However, if the dimensionality of the material is decreased the new variable of length scale becomes available to control the properties of the material [23] due to differences in the density of electronic states. New phenomena are introduced when reducing the tridimensional solid crystalline structures to bidimensional superlattices (see Figure 4) one-dimensional nanowires, or quantum dots, with new opportunities to control S,  $\sigma$  or  $\kappa$ . The introduction of many interfaces in the structure can scatter phonons more effectively than electrons and allows enhanced ZT in such (new) materials. Recent work with PbTe [24]. SiGe [25] and BiSbTe [26.27] superlattices demonstrated an enhancement of ZT. Whereas ZT=2.4 and ZT=1.4 were measured in p-type and n-type Bi-Sb-Te superlattices [28], respectively, no equivalent improvement was found yet in Si-Ge superlattices, when compared to bulk the material.



# Figure 4: A thermoelectric pair made of superlattice materials. Each material is composed of alternating layers of two different materials, with thickness in the range of tens of nanometers.

The current efforts concerning the research of thermoelectric materials are focused in the use of nanostructures in thermoelectric applications. In fact, the thin-film technology is helping to increase the efficiency of these devices. In the last decade, new horizons are opening in the thermoelectricity, in the development of microsystems, and in new techniques to make possible to have figures-of-merit, *ZT*, behind the unitary bound (*ZT*>1) [29,30]. The biggest challenge in the current research of thermoelectric materials is the reduction of thermal conductivity, and the use of thin-films techniques is one way to achieve that reduction. Molecular Beam Epitaxy (MBE) and Chemical Vapor Deposition (CVD) are two possible thin-films deposition techniques to achieve thermoelectric materials based on quantum confinement [26,31].

The use of thin-film processes in thermoelectric structures limits the thickness of the deposited films to few micrometers. Using this thickness, the achieved heat-flow density has higher value, compared with traditional large scale devices. If 10 Wcm<sup>-2</sup> can be found in typical large-scale device then, 500 Wcm<sup>-2</sup> can be supported in a thin-film device. However, this density could not be attended with conventional heatsinks. For lower densities applications, efforts are also being done to achieve bulk materials (rather than films) with increased figures-of-merit. A periodic structure is the major mechanism to reduce the thermal conductivity and to support the enhanced figure-of-merit in superlattices. However, nanocomposites become a natural step for extending the success in superlattices to more scalable materials. Randomly distributed nanostructures in nanocomposite materials (see Figure 5) can lead to a reduction in the thermal conductivity below that of an alloy of the same overall chemical stoichiometry [32]. These materials can be prepared by either wet-chemistry, ball-milling or by inert-gas condensation methods. The nanometer or micrometer sized particles are then hotpressed to obtain dense and mechanically strong, bulk nanocomposites.





#### 2 Thermoelectric converters models

Since each thermoelectric pair can produce a voltage near 1.46  $\mu$ VK<sup>-1</sup>, many pairs connected in series, are necessary to generate a usable voltage. The maximum power in a thermoelectric generator, calculated with equation 5, is obtained when the load resistance equals the internal resistance, *R* [ $\Omega$ ]. Such a power is:

$$P_{MAX} = \frac{V_{OUT}^2}{4R} = \frac{[n(\alpha_p \alpha_n) \Delta T]^2}{4n(R_+ + R_+ + R_+ + 4R_-)}$$
(5)

where *n* is the number of thermoelectric elements (pairs of thermoelectric p-n junctions),  $\alpha [\mu V K^{-1}]$  is the Seebeck coefficient,  $\Delta T [K]$  is the temperature difference between the hot side and cold side of thermoelectric elements and  $R [\Omega]$  is the internal electric resistance of the thermoelectric device. The indexes *p* and *n* refer to p-type and n-type materials respectively and the indexes *j* and *c* refer respectively to materials of contacts and the contact itself. To obtain maximum power, it is also important to match the thermal resistance of the generator with the heatsink (on the cold side) and hot object (in the hot side), not represented in the previous equation . In several

applications, it is also important to analyze the impact of the generator in the temperature of the hot object. If a human body generator is designed then, it will not suit comfortable if much thermal power is absorbed from the skin (the sensation of cold will be noticed). By other hand, when designing a thermoelectric generator for waste heat recovering (e.g., recovering heat from a laptop CPU), an increase of temperature could occur where the heat is generated.

The efficiency of this generator is given by [33]:

$$\phi_{\max} = \frac{q_c}{W} = \frac{T_1}{T_2 - T_1} \times \frac{\sqrt{1 + ZT_M} - \frac{T_2}{T_1}}{\sqrt{1 + ZT_M} + 1}$$
(6)

where Z represents the figure-of-merit of the device, calculated with the help of the equation 7,  $T_1[K]$  and  $T_2[K]$  are the temperatures at hot and cold sides and  $T_M[K]$  is the mean temperature given by  $(T_1+T_2)/2$ . Despite the use of the figure-of-merit to quantify the quality of a thermoelectric material, this parameter is also used to quantify the performance of a thermoelectric device, and it is given by:

$$Z = \frac{(\alpha_p - \alpha_n)^2}{4\kappa\rho_c H} + \frac{8\kappa\rho_c H}{LL_c} + \frac{4\kappa_m\rho H_m}{H} + \frac{8\kappa_m\rho_c H_m}{LL_c} + \frac{4\rho\gamma Ll}{H} + \frac{8\rho_c\gamma l}{L_c}$$
(7)

where, L [m] and H [m] are respectively the length and the height of thermoelectric materials,  $L_c$  [m] is the length of contacts between the thermoelectric material and the metal pads,  $\ell$  [m] is the length of cold area,  $\alpha$  [ $\mu$ Vm<sup>-1</sup>] is the Seebeck coefficient,  $\rho$  [ $\Omega$ m] is the electrical resistivity,  $\kappa$  [Wm<sup>-1</sup>K<sup>-1</sup>] is the thermal conductivity and  $\rho_c$  [ $\Omega$ m] is the contact electrical resistivity. The device is supported by an isolating membrane with thickness  $H_m$  [m] and thermal conductivity  $\kappa_m$  [Wm<sup>-1</sup>K<sup>-1</sup>]. The quantity  $\gamma$  [Wm<sup>-2</sup>K<sup>-1</sup>] represents a coefficient to the include radiation and convection losses, and it is normally in the range 5<><10 Wm<sup>-2</sup>K<sup>-1</sup>.

The maximum temperature difference,  $\Delta T_{max} = (T_h - T_c)_{max}$  [K], between the hot and the cold sides without external load ( $Q_L = 0$ ) can be obtained:

$$\Delta T_{\max} = \frac{ZT_c^2}{2} \tag{8}$$

This maximum temperature difference is obtained when the current, I [A], has a specific value  $I_{out}$  [A], such that  $\partial T_c/\partial I=0$ . Under this condition, such a current is:

$$\frac{\partial T_c}{\partial I} = 0 \quad \leftrightarrow \quad I_{opt} = \frac{(\alpha_p - \alpha_n)T_c}{R} \tag{9}$$

The next step is the minimization of the temperature on the cold side, whose value is:

$$T_c = \frac{\sqrt{1 + 2ZT_h} - 1}{Z}, \quad I = I_{opt}$$
(10)

The previous equations help to predict the effect of reducing the dimensions of a planar thermoelectric device, when the scaling from millimeters to micrometers is done. The graph of the Figure 6 presents the effect of scaling down the dimensions of devices in the XY plane. The scale factor f=1 (in the horizontal axis) represents a device with dimensions L=W=1 mm, H=10 µm and  $H_m=10$  µm. Lower values of *f* represents devices where the dimensions (*L* and *W*) were reduced by a factor *f*.



Figure 6: The effect of scaling the device in the XY plane. The heights of the device and of the support membrane are constant (*H*=10 μm, *H*<sub>m</sub>=10 μm), while the other dimensions are scaled by the value on the horizontal axis.

Since the losses by radiation and convection are less relevant in lower dimension devices, the figure-of-merit increases when the device is smaller. However, a low contact resistivity must be ensured, to keep this higher figure-of-merit. Considering both effects, an optimum dimension exists where the figure-of-merit is maximized.

The Figure 7 presents the complete model of a thermoelectric device [14], including the thermal and the electric domains. This thermoelectric model is for microcooling applications (where the Peltier effect is present). The electrical model (on the left of the Figure 7) includes the electrical equivalent resistance of the device,  $R [\Omega]$ , a voltage source that provides power to the device and a voltage source modelling the Seebeck effect of junctions – given by  $(a_p - a_n)(T_h - T_c)$ . The resultant current is  $I_e$  [A]. On the right side of the Figure 7, the thermal model is presented. The two current sources,  $(a_p - a_n)I_eT_c$ and  $(a_p - a_n)J_eT_h$ , represent respectively the cooling and the heating by Peltier effect. The capacitors  $C_{Lc}$  [F] and  $C_{Lh}$  [F] are the heat capacity on the cold and the hot sides. The resistances  $R_{Lc}$  [Q] and  $R_{Lh}$  [Q] are the losses by convection and by radiation to the ambient temperature ( $T_a$  [K]). The resistance between the hot side and the cold side, including support membrane effects. The variables  $Q_j$  [J] and  $Q_{Jc}$  [J] represent the heating by Joule, respectively in the thermoelectric materials and in the contacts. The load applied on the cold side of the device is represented by  $O_L$  [J].

A thermoelectric cooler can be analyzed using finite element modeling. After designing the structure, two types of loads are considered: the first one is due to the Peltier effect on the hot and cold sides, whereas the second is due to the joule heating.



Figure 7: The complete model of a Peltier microcooler, including electrical and thermal domains.

## 2.1 Peltier effect on hot and cold sides

The cooling by Peltier effect is calculated with the equation 11 and the heating with the equation 12 ( $T_C$  represents the temperature on the cold side and  $T_H$  the temperature on the hot side):

$$Q_c = Q_{nc} + Q_{pc} = (\pi_n + \pi_p)I = (\alpha_p - \alpha_n)I_c \cdot I \quad [J]$$
(11)

$$Q_{h} = Q_{nh} + Q_{ph} = (\pi_{n} + \pi_{p})I = (\alpha_{p} - \alpha_{n})T_{h}I \quad [J]$$
(12)

This load is applied on p-n junction of the device.  $Q_C$  should be negative, since heat is removed from the cold side of the device.

#### 2.2 Joule heating

The joule heating should be considered in all electrical resistances of the device. This includes the p- and the n-type materials, the metallic contact between them and the interface contact resistances. The metallic contact resistance is usually neglected, since this value is very small compared with those found on p- and n-type materials, due to its low resistivity. *W* is the width of elements and the other symbols are as defined in the equation 7. The total equivalent resistance of a thermoelectric n-p pair is:

$$R_{eq} = R_e + 2R_c = \frac{\rho_n L_n}{W_n H_n} + \frac{\rho_p L_p}{W_p H_p} + 2(\frac{\rho_{cn}}{L_c W_n} + \frac{\rho_{cp}}{L_c W_p})$$
(13)

The joule heating should be calculated and applied in these volumes. The convection and the radiation should be considered in all surfaces. The Figure 8 shows the surface temperature of a planar Peltier microcooler, on top of a Kapton polyimide substrate. A temperature difference of 16 K (between the hot side and the cold side) was obttained in simulations [35].



Figure 8: FEM simulation of a microdevice shows the possibility of achieving a temperature difference between hot and cold sides of 16 °C (or 16 K).

# 3 Thin-films technology for thermoelectric materials

The way how materials are deposited is not a pacific issue, and the following example shows exactly this problem. Considering a single junction of a n-p thermocouple having a Seebeck voltage of only 400  $\mu$ VK<sup>-1</sup>, thus, to achieve an usable voltage in generator devices, more than 4000 thermocouples must be connected in series. If these 4000 thermocouples are to be fitted in a 1 cm<sup>2</sup> device then, the size of each thermocouple is about 100  $\mu$ m × 200  $\mu$ m. This means that the fabrication methods used in macro-sized thermoelectric devices cannot be used in these micro-devices. The materials can be deposited by thin-film deposition processes (physical and chemical vapour deposition or electrochemical deposition).

Another controversial issue is the material type to fabricate the thermoelectric structures. The Figure 9 shows the figure-of-merit,  $Z[K^{-1}]$ , calculated for different materials at different temperatures [36] and helps to understand this problem.

Of the great number of materials investigated, those based on bismuth telluride, lead telluride and silicon-germanium alloys emerged as the best for operating at temperatures near 300 K, 900 K and 1400 K respectively. Near the room temperature (250-350 K), tellurium (Te), bismuth (Bi), antimony (Sb) and selenium (Se) composites show the highest figure-of-merit values. For this reason, they are used in many of the commercial Peltier devices. The typical thermoelectric properties at room temperature of some of these materials are displayed in the Table 1 (the nickel, chromium, bismuth, antimony, n-doped silicon-germanium, p-doped silicon-germanium, n-type material bismuth telluride, and p-type material antimony telluride, respectively). For operation at temperatures around 800 K, lead antimony telluride shows the highest figure-of-merit. A ZT value around 1 was reported at 800 K [37]. However, there are environmental

restrictions to the use of lead. Silicon-Germanium is a candidate material for operation at temperatures above 1000 K. A figure-of-merit around unity was achieved at 1200 K [38]. These materials also have the advantage of easy integration with microelectronics.



Figure 9: The figure-of-merit, Z [K<sup>-</sup>], calculated for different materials at different temperatures [36].

Table 1: The thermoelectric properties of some materials.

Material	α [μVK <sup>-1</sup> ]	ρ[μΩ.m]	$\kappa$ [W.m <sup>-1</sup> K <sup>-1</sup> ]	ZT	Temp. [K]
Ni	-18	0.07	91	0.015	300
Cr	18	0.13	94	0.008	300
Bi	-60	1.15	8.4	0.11	300
Sb	40	0.42	18.5	0.062	300
Si-Ge (n)	-242	17.8	4.2	0.94	1200
Si-Ge (p)	240	31.9	4.38	0.5	1200
$Bi_2Te_3(n)$	-240	10	2.02	0.86	300
$Sb_2Te_3(p)$	92	3.23	1.63	0.48	300

Due to its compatibility with IC technology, polycrystalline SiGe alloys and polycrystalline Si are commonly used in thermopile applications. Their use in microcoolers has been investigated, however, their performance is very low compared to that of tellurium compounds, which have been used for many years in conventional large-area Peltier devices [14]. Tellurium compounds (n-type bismuth telluride, Bi<sub>2</sub>Te<sub>3</sub>) are well-established room temperature thermoelectric materials and are widely employed by the industry, in conventional thermoelectric generators and coolers. Several deposition techniques have been investigated for their suitability for fabricating thin-films materials. The direct evaporation of the bulk materials for the deposition of Bi<sub>2</sub>Te<sub>3</sub> films was demonstrated

by Da Silva to be non-suitable. The large differences in vapour pressure of bismuth and tellurium, result in a compositional gradient along the thin-film thickness [32]. Other techniques explored for the deposition of  $Bi_2Te_3$  thin-films are thermal co-evaporation [39], electrochemical deposition [40], co-sputtering [3], flash evaporation [41] and metal-organic chemical vapour deposition (MOCVD) [42]. Although all these approaches are in principle suitable, the co-evaporation was used in this work to obtain both n-type  $Bi_2Te_3$  and p-type  $Sb_2Te_3$  thin-films, because it allows to precisely control the estequiometry of the deposited thin-film with the lowest costs. Only MOCVD is better than the co-evaporation to obtain thin-films with good uniformity and with the desired estequiometry. However, in order to do the deposition of thin-films by MOCVD, a reactor chamber is needed. Thus, this process is too expensive and it requires additional security procedures, when compared with co-evaporation [43].

The influence of deposition parameters on the thin-film performance was analysed in detail. For obtaining data that was statistically significant, more than one hundred samples were fabricated. One essential parameter in the fabrication of thermoelectric microdevices is the film-to-substrate adhesion. To investigate this issue three different substrate materials have been used: glass, silicon and polyimide (kapton). However, for actual thermoelectric applications, a kapton film was chosen as substrate, because of the low thermal conductivity (0.12 Wm<sup>1</sup>K<sup>-1</sup>). Moreover, the thermal expansion coefficient ( $12 \times 10^{-6}$  K<sup>-1</sup>) closely matches the thermal expansion coefficient of the telluride thin-films, thus reducing residual stress and increasing the adhesion. The information obtained on silicon and glass is important for MEMS-based thermoelectric devices, where micromachining is applied for thermal definition of the microstructure. Flexible substrates enable the integration with many novel types of devices, however, also introduce complications, such as the uncommon mechanical properties of the composite film-substrate.

# 3.1 Bismuth and antimony tellurides depositions

Two different approaches can be used for on-chip integration of thermoelectric (TE) devices: transversal (off-plane or vertical) and lateral (in-plane), depending on the direction in which heat is transported, relative to the surface of the device. This fabrication examples felt on the lateral heat flow approach, due to its easier fabrication process and compliance with planar technology [44]. The Figure 10 shows a process flow used for fabricating thermoelectric converters. The fabrication steps are as follows: a thin-layer of metal (aluminium - Al) is deposited by a direct current (DC) sputtering on a polyimide substrate. Then, the patterning of the metal layer is done, and the contacts are obtained (a). Next, the n-type Bi<sub>2</sub>Te<sub>3</sub> thin-film is deposited by thermal co-evaporation (b). The next step starts with the deposition of a negative photoresist (PR) layer, followed by an expose to UV (ultra-violet) light with a mask made of glass and nickel (to block the UV light) placed between the PR and the UV light source. After the exposition to the UV light, the UV-protected areas will be removed during the PR development (c). The n-type elements are patterned by photolithography (d). The n-type thin-film is etched in HNO3 and p-type Sb2Te3 thin-film is deposited by thermal co-evaporation (e). A new layer of PR is deposited, exposed to a UV light source and developed (f). The thermoelectric layer made of Sb<sub>2</sub>Te<sub>3</sub> is patterned by wet etching in HNO3: HCl bath (g) and finally, the PR is removed (h). A protective layer of silicon nitride (Si<sub>3</sub>N<sub>4</sub>) can also be deposited by low-temperature hotwire chemical vapour deposition (HW-CVD) and patterned if required by the application.



The thermoelectric thin-film structures were deposited by thermal co-evaporation (see the deposition setup in the Figure 11) with the help of a high-vacuum chamber (with the base pressure settled to about  $1.33 \times 10^{-4}$  Pa). Two large molybdenum boats (baffled boxes, with a volume of 4 cm<sup>3</sup>) were used at the same time, one for each of the elementary materials required to produce the desired compound. The power applied to

each boat is controlled independently, using two computed proportional-integral derivative (PID) controllers [45] to maintain the deposition rate at user-defined constant values, during the deposition process. Two thickness monitors (quartz crystal oscillators) are carefully placed inside the chamber in such a way that each of them receives material only from the boat it is monitoring. A metal sheet is placed between the two boats to ensure deposition of a material at the respective quartz crystal sensor only. Substrates are heated to the temperature set point,  $T_{sub}$  [°C], in the range 150-270 °C.



Figure 11: The system used in the co-evaporation.

The graphs showing the influence of the evaporation rate, *R*, of each material on thermoelectric properties of the compounds are presented in Figure 12. The evaporation flow rate ratio,  $R=Fr_{Te}/Fr_{Bi,Sb}$ , is defined as the amount (in volume of the deposited film) of tellurium (Te) divided by the amount of bismuth (Bi) - or antimony (Sb) - that arrives the substrate during deposition. The highest power factor (PF) was obtained with a Bi (or Sb) evaporation rate of 2 Ås<sup>-1</sup> and a Te evaporation rate of 6-7 Ås<sup>-1</sup>, which corresponds to an evaporation flow rate ratio in the range 3-3.5.



Figure 12: The power-factor of  $Bi_2Te_3$  (top) and  $Sb_2Te_3$  (bottom) thin-films as a function of the Te/Bi evaporation flow rate ratio, R, and the respective curve fittings (solid lines).

The best values of  $T_{sub}$  for Bi<sub>2</sub>Te<sub>3</sub> and for Sb<sub>2</sub>Te<sub>3</sub> thin-films were about 270 °C and 220°C, respectively. Finally, it must be noted that all thin-films were deposited on a polyimide (kapton) foil with a thickness of 25  $\mu$ m. The Figure 13 shows two SEM cross-section and surface images of both Bi<sub>2</sub>Te<sub>3</sub> and Sb<sub>2</sub>Te<sub>3</sub> thin-films, where their polycrystalline structure can be confirmed. Also, the former temperatures and the optimal evaporation flow rate ratios, *R*, were those which resulted in thin-films with larger grain size. This is of major concern, because a crystalline structure with an increased grain size is less resistive, whose consequence is a thin-film with an increased thermoelectric figures-of-merit, *ZT*.



Figure 13: SEM top view (left) and cross-sectional (right) images of Bi<sub>2</sub>Te<sub>3</sub> (top) Sb<sub>2</sub>Te<sub>3</sub> (bottom) thin-films.

# 3.2 Optimization of thermoelectric properties

The in-plane thin-film electrical resistance was measured using the conventional four probe van der Pauw method, at room temperature. The thermal conductivity  $[Wm^{-1}K^{-1}]$  was measured using the method proposed by Völklein [46], and vales of 1.3  $Wm^{-1}K^{-1}$  and 1.8  $Wm^{-1}K^{-1}$  were obtained for the Bi<sub>2</sub>Te<sub>3</sub> and Sb<sub>2</sub>Te<sub>3</sub> thin-films (which were deposited as conditions to obtain the maximum power-factor), respectively. The measurements of the Seebeck coefficient were made, by connecting one side of the thin-film to a fixed temperature (heated metal block) and the other side to a heat sink at room temperature.

The Figure 14 shows a X-ray diffraction (XRD) spectrum of the best Bi<sub>2</sub>Te<sub>3</sub> (top plot) and Sb<sub>2</sub>Te<sub>3</sub> (bottom plot) thin-film, which reveal their polycrystalline structures. The peaks agree with the diffractograms for polycrystalline Bi<sub>2</sub>Te<sub>3</sub>. The peaks also agree with the power diffraction spectra for polycrystalline Sb<sub>2</sub>Te<sub>3</sub>. The peaks also agree with the power diffraction spectra for polycrystalline Sb<sub>2</sub>Te<sub>3</sub>. The Tables 2 and 3 show the most important thermoelectric characteristics obtained from the measurements applied on the best samples of Bi<sub>2</sub>Te<sub>3</sub> and Sb<sub>2</sub>Te<sub>3</sub> thin-films. The measurements done in the best samples show an absolute value of the Seebeck coefficient in the range of 91-248  $\mu$ VK<sup>-1</sup>. An in-plane electrical resistivity of 7.6-39.1  $\mu$ Ω.m was obtained. The measurements for the Bi<sub>2</sub>Te<sub>3</sub> and Sb<sub>2</sub>Te<sub>3</sub> thin-films also reveal figures-of-merit, *ZT*, of 0.97 and 0.56, and power-factors, *PF*, of 4.87×10<sup>-3</sup> WK<sup>-1</sup>m<sup>-2</sup> and 2.81×10<sup>-3</sup> WK<sup>-1</sup>m<sup>-2</sup>, respectively.



Figure 14: XRD analysis of  $Bi_2Te_3$  (top plot) and  $Sb_2Te_3$  (bottom plot) thin-film analysis. In the both plots, the peaks agree well with the respective power diffraction spectrums (doted lines and diamonds).

Fable 2: P	roperties of	the best	samples of	Bi>Te3	thin-films.
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TF	T <sub>sub</sub> [°C]	R	%Te by EDX	α [μVK <sup>-1</sup> ]	ρ[μΩm]	<i>PF</i> [WK <sup>-2</sup> m <sup>-1</sup> ]	<i>ZT @</i> 300K
#1	190	1.70		-180	16.6	1.95×10 <sup>-3</sup>	0.39
#2	230	2.10	62.8	-156	11.3	2.16×10 <sup>-3</sup>	0.43
#3		3.10	62.2	-152	13.4	1.72×10 <sup>-3</sup>	0.34
#4	240	3.20	59.1	-180	16.6	1.95×10 <sup>-3</sup>	0.40
#5	270	3.20	62.0	-248	12.6	4.87×10 <sup>-3</sup>	0.97
#6		3.90	_	-220	10.6	4.57×10 <sup>-3</sup>	0.91

Га	b	le .	3:	Pro	perties	of	the	best	samp	les	of	Sb	$_2T$	ſe3	thin-	-fil	lm	¢
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TF	T <sub>sub</sub> [°C]	R	%Te by EDX	α [μVK <sup>-1</sup> ]	ρ [µΩm]	<i>PF</i> [WK <sup>-2</sup> m <sup>-1</sup> ]	<i>ZT @</i> 300K
#1	150	1.47	54.5	91	7.6	1.09×10 <sup>-3</sup>	0.22
#2		1.67	61.4	140	14.0	1.40×10 <sup>-3</sup>	0.28
#3	180	2.02	59.1	158	30.3	0.82×10 <sup>-3</sup>	0.16

1	#4		2.35	62.4	156	39.1	0.62×10 <sup>-3</sup>	0.12
	#5	220	2.50	67.3	156	9.2	2.66×10 <sup>-3</sup>	0.53
	#6		3.18	73.5	188	12.6	2.81×10 <sup>-3</sup>	0.56

#### 4 Superlattices for fabrication of thermoelectric converters 4.1 Why superlattices?

The dimensionless thermoelectric figure-of-merit, ZT, in bismuth/antimony/telluride bulk alloys has remained around the unity for more than 50 years. The best results up to now showed that a peak ZT of 1.4 at 100°C could be achieved in a p-type nanocrystalline BiSbTe bulk alloy [47]. Such nanocrystalline bulk materials were made by hot pressing nanopowders that were ball-milled from crystalline ingots under inert conditions. Also it was observed that the ZT improvement was the result of low thermal conductivity caused by the increased phonon scattering by grain boundaries and defects. But the most important result was a ZT of about 1.2 at the room temperature and 0.8 at 250 °C, making these materials useful for cooling and power generation [47]. However, the obtainance of these materials is not an easy task, because nanocrystalline structures must be obtained (see the Figure 5).

The superlattices are an alternative but simpler way to improve the thermoelectric characteristics of the structures, because it is only need to alternate layers of two different materials with thickness in the range of tens of nanometers (see the Figure 4). Previous work [27] demonstrates that superlattices can be fabricated by CVD deposition of alternating layers. However, the cluster formation during the deposition of few nanometers can avoid a homogeneous film thickness. A low substrate temperature is used to improve the thickness homogeneity of the thin-films.

## 4.2 Materials and properties

In order to enhance the ZT, a high Seebeck coefficient, an increased electrical conductivity, and a decreased thermal conductivity are needed, but the conventional bulk materials properties often counter each other [48]. Because the performance of thermoelectric devices is determined by the figure-of-merit, ZT, of the thermoelectric device, both the superlattice structure and the device must be optimized in the design and the fabrication process [49]. There are available thermoelectric structures made of InGaAs/InGaAsP superlattices and such study had proven that the superlattice at a certain periodic length has minimal thermal conductivity, which, in general, corresponds to an enhanced ZT [49].

Superlattices with improved thermoelectric figures-of-merit, ZT, were also fabricated by several research teams around the world. These thermoelectric structures can be made with materials such as  $B_{12}Te_3/B_2Te_3/B_12E_3/B_12$ 

## 4.3 Fabrication

A huge number of conventional techniques already used by the microelectronics industry can be successfully applied for fabricating thermoelectric devices. Such techniques include the photolithography, electroplating, wafer dicing, and pick-andplace systems. This allows the fabrication of a wide spectrum of thermoelectric devices that range from the simple modules for handling a few microwatts [58] (in cooling or energy conversion) to more complex module arrays (to handle higher power levels) [59].

The quality of the deposited thin-films (either both constitutive layers or the entire superlattice) must be high in order to successfully fine-tuning the thin-film thicknesses in a superlattice so as to hinder lattice vibrations (thus decreasing heat flow) and transmit electrons (increasing electrical conductivity), using materials that intrinsically have a large thermopower; this generates a thermoelectric material with a particularly high figure-of-merit [60]. The conventional imaging techniques based on X-rays diffractions don't offer satisfactory resolution to make a quality assessment of the surface of the deposited thin-films. In this context, the Scanning Probe Microscopy (SPM) technique fills such a gap, because high-resolutions of a few picometres can be obtained. This is due to the resolution to be only dependent of the size of the probe-sample interaction volume [61].

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