Chapter 2
Microsystems for Wireless Sensor Networks with Biomedical Applications

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ABSTRACT

This chapter introduces the concept of wireless interface, followed by the discussion of the fundamental items, concerning the fabrication of microsystems comprising low-power devices. Using as example, a design of a RF transceiver the frequency of 2.4 GHz and fabricated using a UMC RF CMOS 0.18 μm process, it will be discussed the main issues in the design of RF transceivers for integration in wireless microsystems. Then, it will be presented two biomedical applications for wireless microsystems: the first is a wireless EEG acquisition system, where it is presented the concept of EEG electrode and the characterisation of iridium oxide electrodes. The other application, is a wireless electronic shirt to monitoring the cardio-respiratory function. The main goal of these applications, is to improve the medical diagnostics and therapy by using devices which reduces healthcare costs and facilitates the diagnostic while at the same time preserving the mobility and lifestyle of patients.

1 WIRELESS INTERFACES AND MICROSYSTEMS

1.1 Introduction

Wireless communication microsystems with high density of nodes and simple protocol are emerging for low-data-rate distributed sensor network applications such as those in home automation and industrial control. This type of wireless microsystem with sensors and electronics are becoming of interest for biomedical applications. Moreover, in order to implement an efficient power-consumption wireless sensor it is necessary to develop a low-power low-voltage RF CMOS transceiver. As is of common knowledge, the CMOS technology has reached its maturity. Therefore, design engineers used it for developing RF circuits. The advantages of CMOS technology are the higher integration, low-power consumption, low-voltage supply and low-cost compared with Bipolar technology. The use of CMOS process with low length for the channels of the MOSFETs is very important for high-frequency devices. As will be seen further in this chapter, this was one of the main reasons that were behind the choice of the UMC RF 0.18 μm CMOS process to design, optimise and fabricate, a radio-frequency (RF) transceiver for the operation in the frequency of 2.4 GHz.

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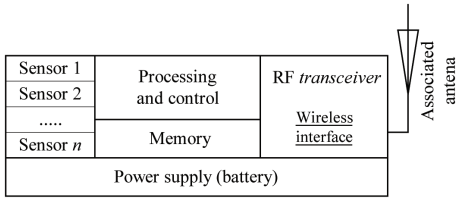
Figure 1. A generic microsystem architecture, which connects to an associated antenna

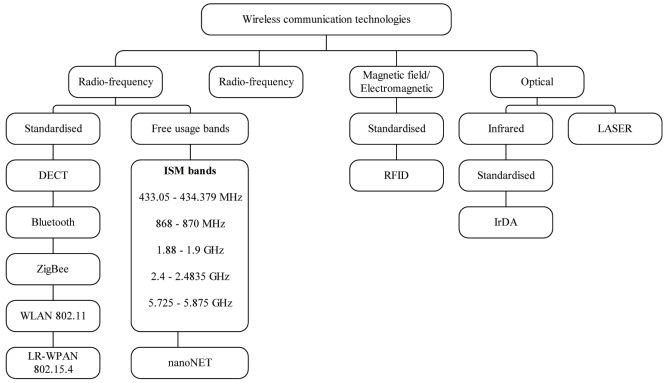


1.2 System Requirements

In wireless sensors networks, the communication is made by way of a radio-frequency (RF) link. Thus, in order to such a communication be possible, a wireless interface must be designed. This wireless interface is a RF transceiver, which after be connected to an associated antenna, makes possible to wirelessly communicate with the exterior. The RF transceiver must present dimensions comparable with the other elements of the microsystem, in which it will be integrated, such as the sensors and the electronics of processing and control. Miniaturised microsystems makes possible to have mass productions with low prices, favouring the spread of applications relying on these same microsystems. Moreover, solutions relying in wireless microsystems, offer a flexibility such as it is possible to chose how many and which are the sensors to be integrated together with the RF transceiver and the remain electronics. Using multi-chip-module (MCM) techniques and a limited number of components in different technologies, it is possible to fabricate devices for a huge range of applications. Figure 1 shows a generic microsystem architecture for use in wireless sensors networks applications. This microsystem connects to an antenna and it is given a special focus to the way the different blocks interact between each other.

In wireless communications, the antenna is one of the most critical subsystem, thus, in order to not compromise the desired miniaturisation, the antenna must be small enough to comply with size constraints of the microsystems. The investigation of new frequency bands (Celik *et al*., 2008) and new geometries (Mendes *et al*., 2006) will make possible to have smaller antennas to integrate in wireless microsystems (Touati & Pons, 2003; Carmo *et al*., 2006). This makes the chose of the most suitable frequency, one of the more decisive aspects in the design of RF transceivers. Normally, the desired range, baud-rate and power consumptions are key-aspects in the design to take in account, when the frequency of operation is to be selected. At a start-up point, the range limits the maximum usable frequency, because the loss suffered by the radiowaves in the free-space increases with the distance. Considering the loss for a line-of-sight (LOS) scenario (Lee & Lee, 2000):

Figure 2. Available frequency bands and respective applications



$$a = [\lambda/(4\pi d)]^2 \quad (1)$$

where, λ is the wavelength [m] and d [m] is the separation between the transmitter and the receiver, thus anyone concludes that a way to compensate the loss due to an increase in the distance, is to increase the transmitted power. However, to keep or even increase the useful life of the batteries, such a variation in the transmitted power is not possible to do. Moreover, in the case of applications requiring higher baud-rates, the transmitted bandwidth must also be higher, in order to support these applications. However, the frequency can't be arbitrarily increased, because this have implications in the power consumptions, e.g., at high frequencies, the transistors must switch faster compared with the operation at lower frequencies, thus the energy dissipation is bigger.

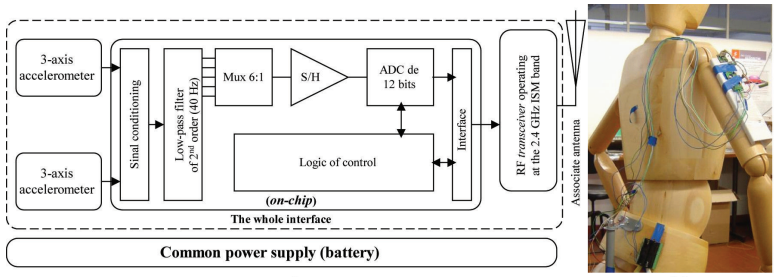
Figure 2 shows the available frequency bands for the different technologies used in wireless communications. The most suitable frequencies are those belonged to the so called ISM band (Industrial, Scientific and Medical), due to its unregulated usage, e.g., these frequencies are not subjected to standardisation and can be freely used, since the emitted power are maintained below the maximum levels imposed by the legislation. Such a flexibility leaded to the rising and spreading of interesting applications.

1.3 Applications

Figure 3 shows the block diagram and the respective interface for monitoring the body movements of individuals. This interface connects to a set of accelerometers with three axis, which are used to measure the relative position of members to the thorax. The interface uses an analog multiplexer followed by an analog-to-digital converter (ADC) to acquire and process the signals. All of the analog electronics of control and processing is managed using the control logic of the interface. A RF module from the company Crossbow, uses a wireless link at the 2.4 GHz frequency, to exchange data (Crossbow, 2009).

Higher frequencies such as those in the range 5.7-5.89 GHz makes possible to have antennas sufficiently small, in order to fabricate microsystems, containing the wireless interface and

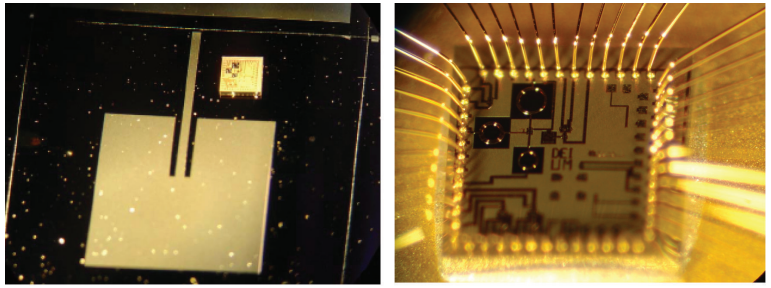
Figure 3. (a) The block diagram of a wireless interface for operation at the 2.4 GHz ISM band and ready to be used in biomedical applications, and (b) an interface already mounted in the arm of a test-dummy



antenna. Moreover, these kind of solutions helps to reduce the problems related to impedance mismatches, while at the same time, it increases the systematisation of the manufacturing processes and delivers microsystems with an even reduced price (Callaway Jr., 2004). Figure 4 (a) shows a microsystem, where it can be seen the RF transceiver mounted together with a chip-size antenna of planar type, which were optimised and fabricated for the operation in the 5.7 GHz ISM band and measures 7.6 × 7.7 mm (Carmo *et al*., 2006). The microdevice shown in Figure 4 (b), is the RF transceiver used for the transmission at 5.7 GHz

A wireless module specially designed to be compatible with IEEE 802.15.4 (a specific protocol for wireless sensor networks applications) is proposed in (Choi *et al*., 2003). Such a modules has two microdevices mounted in a board with a square area of 9 mm^2. One of the microdevices is a RF transceiver operating at 2.4 GHz with power consumptions of 21 mW and 30 mW when it is put

Figure 4. (a) Chip-size antenna for operation at 5.7 GHz assembled with a RF transceiver and (b) a magnified photograph of the same RF transceiver (Carmo et al, 2006)



to receive or to transmit, respectively. The other microdevice makes the base-band processing and has internally a modem to have reliable and error-free data communications between the transmitter and the receiver. This second microdevice has also an internal processor with capacity of storage. The management and the interoperacionality of all subsystems of this microdevice is made by way of an internal processor. Both microdevices were designed and fabricated in a RF CMOS 0.18 µm process.

A microdevice presented in (Enz *et al*., 2005) consists in another low-power solution for wireless sensors networks and was also fabricated in a RF CMOS 0.18 µm process. Internally, this microdevice has a microcontroller of RISC (Reduced Instruction Set Computer) architecture, RAM memory (Random Access Memory), a power supply management system, a RF transceiver, an analog part with a digital-to-analog converter (DAC) for signal conditioning and peripheral circuits to communicate with external devices (SPI and I^2C buses). The electronics of control runs a wireless sensors networks specific protocol: the *WiseMAC*. Such a protocol puts the power consumption thirty times bellow, compared with those it was obtained the chosen protocol it was the IEEE 802.15.4. The RF transceiver offers the possibility to select the operation frequency between the 433 MHz and the 868 MHz, as well as for the used modulation, which can be chosen between OOK (*On/Off Keying*) or *FSK* (*Frequency Shift Keying*). This transceiver consumes 2.5 mW and 39 mW, when it is put to receive or to transmit, respectively.

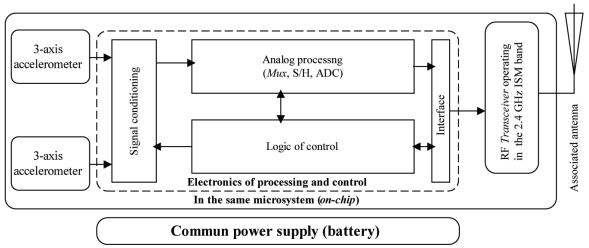
The next application explores two key-factors to reduce the power consumption (Cho & Chadrakasan, 2004). These factors are the start-up and the transmission times. The first one is the time that lasts between an enable order and the instant the electronics starts to work. The second, is the time to send a complete packet of data. The optimisation of these times gives a big contribution in the power consumption reduction of the transmitter. Normally, the nodes for low-power applications has low temporal cycles of working (*duty-cicles*), as well as short packet lengths, thus, the start-up time can have a significant impact in the whole power supply. In the context formerly presented, the transmitter must send the data in the lowest period of time (high baud-rates), while simultaneously must present the lowest start-up time. This solution relies on a transmitter for FSK transmission in the frequency of 6.5 GHz. This transmitter has a start-up time of only 20 µs, which correspond to send 50 bits of information at its maximum baud-rate of 2.5 Mbps.

2 RF CMOS TRANSCEIVER

2.1 Motivation

In wireless sensors networks, the continuous working time of sensorial nodes are limited by its average power consumption (Mackensen *et al*., 2005). Excluding the RF transceiver, the sensors and the remain electronics has no great impact in the power consumption of wireless nodes (Gutierrez *et al*., 2001). In fact, it's well demonstrated that the RF transceiver is the subsystem with the biggest power consumption, in spite to be available a lot of technologies with increased power-consumption efficiencies (Enz *et al*., 2005). The co-definition of new architectures and algorithms is a topic of even more concern, in order to quantify in advance the exact implication of the RF system in the total power consumption (Bicelli *et al*., 2005). To conclude, without proper design, communication will increase network power consumption significantly because listening and emitting are power-intensive activities (Enz *et al*., 2004). Thus, in order to optimise the power consumption, it was designed a RF CMOS transceiver for the operation in the 2.4 GHz ISM band. It was used the UMC RF 0.18 µm CMOS process in the design. This process has one poly and six

Figure 5. In the same microsystem, the integration of a RF transceiver, sensors and electronics



metal layers, allowing the use of integrated spiral inductors (with a reasonable quality factor), high resistor value (a special layer is available) and the low-power supply of 1.8 V.

Moreover, in order to optimise power management, the RF CMOS transceiver design predicts the use of control signals. With these control signals it is possible to enable and disable all the subsystems of the transceiver. These signals allows, e.g., to switch off the receiver when a RF signal is being transmitted, to switch off the transmitter when a RF signal is being received, and allows the transceiver to enter to sleep when RF signals are neither being transmitted, nor being received.

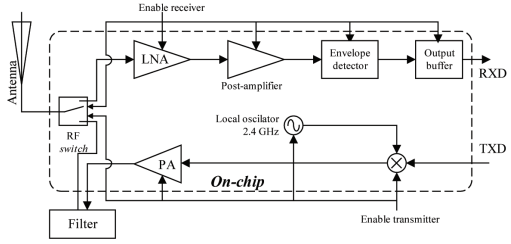
An important feature that the RF CMOS transceiver must allow, is the possibility to be integrated together in the same microsystem with sensors and the remain electronics of processing and control, in order to reduce the number of supply-points (Figure 5). This makes more practical and easy to supply all the subsystems, since it needs to attach a single battery.

2.2 Specifications

Figure 6 shows the block schematic of the RF CMOS transceiver, which consists of a receiver, a transmitter, an antenna-switch and a Phase-locked Loop (PLL) as a frequency synthesiser.

The receiver adopts a direct demodulation, by means of envelope detection. The power budget of the RF link must be made, in order to have in any noise condition and with the maximum baud-

Figure 6. The block schematic of the transceiver



rate of 250 kbps, a bit error probability (BEP) less that 10^{-6} (BEP=$P_e \leq 10^{-6}$). This target quality of service (QoS) is for a maximum transmitted power of 0 dBm (1 mW) with Amplitude Shift Keying (ASK) modulation. Using an antenna with an output impedance of 50 Ω (at the frequency of 2.4 GHz) and a Spectrum Analyser, model *Agilent E4404-B*, it was made several measurements of the environment noise. It was observed that the noise power never crossed above N=-104 dB. The previous known of noise levels and the QoS of the system are mandatory, in order to know the minimum sensitivity of the receiver. From the BEP of ASK with envelope detection (also known as non-coherent ASK systems) (Carlson *et al*., 2001):

$$P_e = \tfrac{1}{2} e^{-\gamma_0/2}, \quad \gamma_0 \gg 1 \tag{1}$$

where γ_0 is the signal-to-noise ratio (SNR) at the receiver and to have $P_e \leq 10^{-6}$, it is necessary a minimum SNR in the receiver site of $\gamma_0 \geq 26$ (γ_0=14 dB). This imposes a minimum signal power, S_{min}, in the receiver such that $\gamma_0 = S_{min} - N \geq 14$ dB. Then, the sensitivity of the receiver must be at least $S_{min} = 14 + N = -90$ dB $\triangleq$ -60 dBm. Starting with the specified transmitted power of P_t=0 dBm $\triangleq$ =-30 dB and applying the free-space loss equation:

$$L_f(d_m) = 20\log_{10}\left(\frac{75}{\pi d_m f_{MHz}}\right) \text{ [dB]} \tag{2}$$

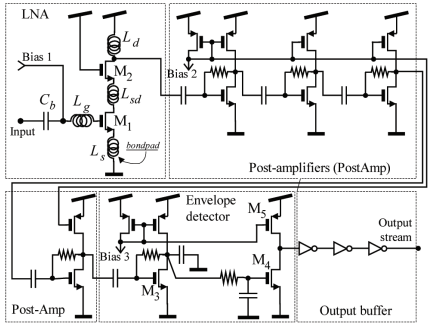
where d_m is the distance (in meters) and f_{MHz} is the frequency (in MHz), the SNR for a ten meters range is such that $\gamma_0 = P_t - L_f(d\text{=}10\text{m}) - N \cong +13.96$ dB. This SNR is very close the required +14 dB with a relative error less than 0.29%, thus it is not necessary to modify the specifications of the transceiver. However, a further theoretical validation must be made, in order to confirm that the noise measurements really met the specifications of the RF transceiver. Let's consider the use of unipolar NRZ (non-return to zero) pulse shaping for ASK transmission and the typical noise level of +22 dBμV/MHz for a large city and/or for ignition noise (Parsons, 2000). This means that the bandwidth of the link can be approximately by the twice of the maximum band-rate (e.g. 2×250 kHz), thus the noise signal will have in this case, a amplitude equal to +11 dBμV, which corresponds a noise voltage of $n = 10^{+11/20} \approx 3.55$ μV. Finally, assuming a perfect matching between the antenna and the receiver, the noise power will be $N = 10.\log_{10}(\tfrac{1}{2}.n^2/50) \approx -129$ dB, which is less of the supra-cited maximum measured value (N=-104 dB). This proves clearly that the noise measurements didn't imply an optimistic sensitivity of the receiver, e.g., there is no risk to break with the specifications.

2.3 Receiver

As shown in Figure 7, the receiver's front-end is a chain composed of a Low-Noise Amplifier (LNA), a post-amplifier, an envelope detector and by an output buffer. The post-amplifier provides additional gain to the RF signal coming from the LNA and the envelope detector senses the presence of the 2.4 GHz carrier. Then, after the envelope detection, the resulted signal is injected in the output buffer, in order to transform it in a perfect NRZ rail-to-rail signal.

For analog blocks, the Figure 8 (a) shows the principle used to switch on and off. The transistors M_{1x} are normally in the cut-off state due to theirs gate-source voltages be zero. However, when a voltage, $V_{control}$ of 1.8 V is applied, they start to conduct; then the current sources constituted by the transistors M_{2a} e M_4 are activated. M_4 behaves like a resistor, thus making the transistors M_{2b}, M_{2c} and further (if more were available) behaving like current sources, e.g., they start to inject current in the branches *Bias* 1 and *Bias* 2. In a same way, the current sources constituted by the transistors M_{5a} e M_3, are also activated, which makes the transistors

Figure 7. The schematics of the receiver



M_{5b}, M_{5c} and further, behaving like sinks. These sinks absorbs the currents which travels from the branches *Bias* 3 and *Bias* 4.

Figure 8 (b) shows the principle to control digital blocks, and it can be seen the addition of the transistor M_3 to the inverter constituted by M_1 and M_2 (Baker *et al*., 1997). Normally, the M_3 is also in the cut-off state, because as in the previous case, its gate-source voltage is also zero, thus the power consumption of the inverter will be zero. Digital drivers with high-impedance outputs applied in digital buses use this same principle, when outputs with high impedance are desired.

2.3.1 Low-Noise Amplifier (LNA)

In a typical receiver, the LNA is the first gain stage in the receiver path, thus, in a LNA, the signal must be amplified as much as possible, with a small signal-to-noise ratio (SNR) decrease. This is achieved with the best (lowest) noise figure (NF).

The LNA is an inductively degenerated common source amplifier (Yao *et al*., 2007). This makes the input impedance at 2.4 GHz equal to 50 Ω, for matching with antenna-switch. As shown in Fig. 10, the cascading transistor M_2 is used to increase the gain, to better isolate the

Figure 8. a) Principle used to enable and disable analog blocks and b) principle used to enable and disable digital blocks

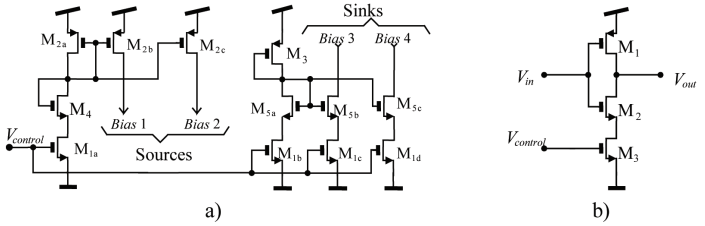
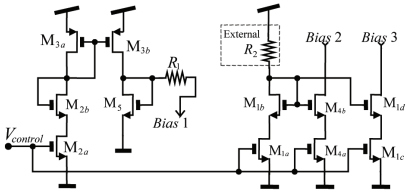


Figure 10. Circuits to bias the stages of the receiver and to activate and deactivate it



output from input and to reduce the effect of M_1's C_{gs}. The LNA is putted in the sleeping mode, by cutting the current in the polarisation stage. The same principle applies to the all subsystems of the transceiver. The inductance L_s is implemented with the bonding connection to the external PCB, which has been calculated to be 0.9 nH/mm (Alimenti *et al*., 2001). The wires used to connect the die to an external PCB, with a RF substrate, has an inductance that adds to the LNA circuit. The inductance L_{sd} helps to overcome a problem associated to the bondingpad effect. This effect appears due to the addition of the inductance in the wire, used to connect the pads in the die circuit to the PCB, with a RF substrate. For this LNA, the input impedance is given by (Martins *et al*., 2008):

$$Z_{in} = sL_g + 1/(sC_{gs}) + [(g_{m1}/C_{gs}) + sL_s] \quad (3)$$

The input matching is made, by trimming the values of the L_s and L_g inductances. The matching is achieved, when the input impedance is real and equal to the impedance, Z_{ant} of the antenna. The most common value is equal to 50 Ω, thus, the two following conditions must be simultaneously verified:

$$\begin{cases} sL_g + sL_s + 1/(sC_{gs}) = 0 \\ (L_s / C_{gs}) g_{m1} = Z_{ant} \quad (= 50\Omega) \end{cases} \quad (4)$$

The start-up point in the LNA design, was the width calculation for the transistor M_1, using the optimal value W_{opt} [μm], given by (Shaeffer & Lee, 2004):

$$W_{opt} = \frac{1}{6\pi f_c L C'_{ox} Z_{in}} \text{ [μm]} \quad (5)$$

where, f_c [Hz], is the working frequency of the LNA; L [μm] is the M_1's length, C'_{ox} [F.m^{-2}] is the oxide per area unit capacitance and finally, Z_{in} is the input impedance of the LNA, which is desired to be purely real and equal to 50 Ω.

The oxide per area unit capacitance is:

$$C'_{ox} = \varepsilon_{ox}/T_{ox} \quad (6)$$

where, T_{ox} [m] is the SPICE parameter, which defines the oxide thickness (UMC 2001). The parameters, T_{ox}=4.2×10^{-9} m and ε_{ox}=4.1ε$_0$=4.1×8.85 aF/μm, presented in the UMC 0.18 μm RF CMOS process, helps to obtain the oxide per area unit capacitance, C'_{ox}=8639.3 aF.μm^{-2}=8.6393 mF.m^{-2}. Thus, the optimal width that simultaneously minimises the consumption and the NF of the LNA, is equal to W_{opt}=284.29 μm. The UMC 0.18μm RF CMOS process has MOSFET optimised to the operation at high frequencies: the RF transistors. For such transistors, the M_1's gate-source capacitance is C_{gs}=830 fF and its transconductance is g_{m1}=20.27 mS. Finally, the values for each of the inductance

are L_s=2.01 nH and L_g=3.27 nH. The most suitable block capacitance at the input of the LNA, is C_b=10 pF. The observed current at the drain of the transistor M_1 is 2 mA. This is the minimum achievable limit for the current supply.

It was predicted as most as possible in the design, the integration of RF components, in order to avoid mismatching problems related to the passive elements of the circuit. This also applies to all DC blocking capacitors. The values of the previous inductances were obtained for a capacitance, C_{gs} for a transistor with an arbitrary width W=W_{opt}. The UMC foundry offers transistors optimised for RF operation, thus, the choice felt on these devices, due to its low-noise and better isolation properties, compared with the use of mixed-mode transistors. The width of such devices can't be any value, in fact, this value depends with the number of fingers in the MOSFETs. For each MOSFET transistor, the maximum number of fingers are twenty one (#21), e.g., the maximum width is limited to 105 μm. This was the first reason to make the width of M_1 equal to 105 μm, against the optimal value W_{opt}. The second reason, deals with the fact to have a small DC block capacitance C_b=2 pF, e.g., it occupies less chip area compared with 10 pF, thus, it's easy to integrate this capacitor with the LNA.

The new value of the parasitic gate-source capacitances of the MOSFETs M_1 and M_2, is C_{gs}=129.94 fF. Thus, taking in account the bondwire inductance (0.9 nH/mm), it results in the internal inductance at the source of the MOSFETs, L_{s_int}=41.2 pH and with the transconductance g_{m1}=21.28 mS. These values are calculated for the drain-source voltage, V_{ds}=1.03 V and for the bias voltage V_{gs}=579 mV. Using the equation (4), it results for the external inductances, L_{s_ext}=0.264 nH and L_g=33.5 nH. It must be noted that L_{s_ext}=L_s-L_{s_int}=R_s.C_{gs}/g_{m1}-L_{s_int}.

The gate inductance was further adjusted to a new value, L_g=21 nH, because it wasn't possible to achieve a satisfactory gain with the previous value. The inductance, L_{sd}, which is connected between the transistors M_1 and M_2, measures 10 nH and is used to increase the gain of the LNA and to improve the S_{11} parameter, by lowering the return-loss at the input. The inductance that connects to the drain of M_2, measures L_d=4.4 nH and is tuned to the 2.4 GHz frequency by means of a 1 pF capacitance. The inductance L_s is below the minimum permitted by the UMC process, thus, it must be made with the use of bondingwires. The inductance L_{sd} is the only one that is not connected to the outside of the die, thus, the remaining inductances must take in account the effect of the bondwire. Then, the actual values of these inductances are slightly smaller than those obtained in the theoretical calculations. Once again, the bondwire with a diameter of 20 μm has an inductance 0.9 nH/mm. The Table I shows the components of the LNA, e.g., the internal inductances and the bondwires (UMC 2002).

2.3.2 Post-Amplifier

Normally, the amplitude of the RF signal at the output of the LNA is not enough to make the envelope detector to work correctly, thus, a post-amplifier is required to provide additional gain. The amplification must be such that for a received power of -60 dBm (the receiver sensitivity), the amplitude of the RF signal at the input of the envelope detector is still enough to make the detection. Thus, in this last case, the voltage at the input of the envelope detector will be always above the 70 mV (Carmo *et al*., 2005).

2.3.3 Envelope Detector

The idea of the envelope detector is as follows: an increasing in the input amplifier implies a decrease in the M_3 gate voltage (this keeps the branch current constant), meaning a decrease in the M_4's gate voltage (after filtering), thus decreasing the transistor M_4 current itself. When this current reaches a point that cancels with the transistor M_5 mirror current, then the output capacitance starts

Table 1. Components of the LNA

	Value 1 [nH]	Q_1	Value 2 [nH]	Q_2
	On-chip	*Inductances*	*Bonding*	*Inductances*
L_s			0.305	20
L_g	18.26	8.249	0.9	20
L_{sd}	10.00	7.177		
L_d	3.145	7.177	0.9	20

to discharge and the output voltage goes to high (Piella, 2001).

This circuit was tested for an input signal modulated in ASK and with an amplitude of 200 mV. It was observed that when the carrier ceases to be present, the output voltage don't decay immediately from 1.8 V to zero. The most severe situation in terms of jitter, is when the data transmission is made with the maximum baud-rate of 250 kbps. In this situation, the observed jitter don't exceeded 20 ns, which corresponds to only 0.005 bits.

2.3.4 Output Buffer

The connection of an excessive capacitance load at the envelope detector, can make severe distortions in the waveshape at the output of this detector. Moreover, the external static electricity can damage or even destroy the circuit of the receiver. A solution to overcome these two problems, is to put a more effective and reliable circuit: the output buffer, whose schematic is depicted in Figure 9.

It was measured the effect of connecting the output of the die to an external circuit with unity gain. In these measurements, it was used the Texas Instruments integrated circuit, TLC082. Under this scenario, the input load is equivalent to a parallel of a 20 pF capacitance with a resistance of 100 kΩ (Texas Instruments, 2009). It was observed, that even in the worse situation, e.g. transmitting at the maximum baud-rate of 250 kbps, the wave at the output of the die didn't suffered almost any kind of distortion.

2.3.5 Bias Circuitry

The schematic shown in Figure 10 illustrates all the bias distribution system, which uses the common signal, $V_{control}$, in the activation of the receiver. Normally, the voltage at the point *Bias* 1

Figure 9. The schematic of the output buffer

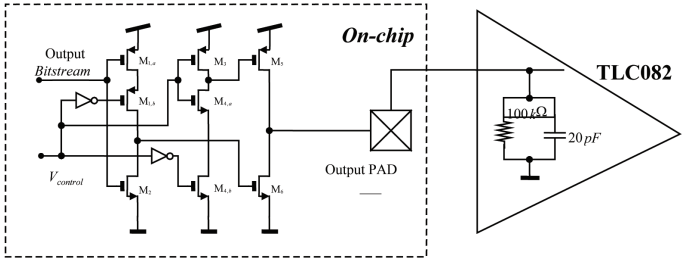


Figure 10. Circuits to bias the stages of the receiver and to activate and deactivate it

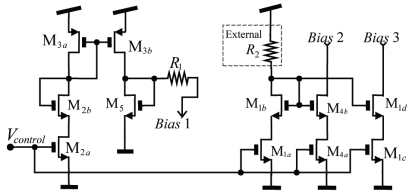
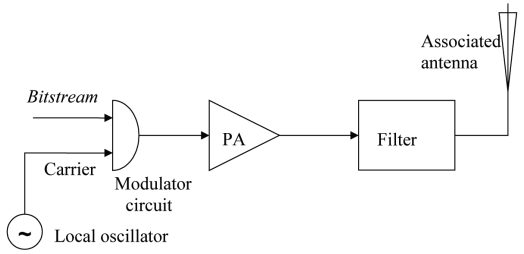


Figure 11. The block diagram of the transmitter



is floating, thus the gate of the transistor M_1 shown in Figure 10 is also electrically floating and the LNA is disabled. When the control signal, $V_{control}$, changes from zero to 1.8 V, the LNA switch to the on state and starts to amplify.

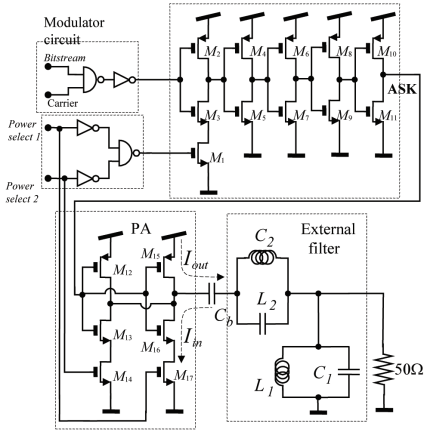
The post-amplifier and the envelope detector remain in the off state, when the control signal, $V_{control}$, still be zero. In this case, the transistor M_{1a} (Figure 10) is in the cut-off state and the same applies to the transistor M_{1b}, then also the transistors M_{4a}, M_{4b}, M_{1c} and M_{1d} are in the cut-off state. When this happens, no current is drained from the *Bias* 2 and *Bias* 3, thus it makes that both the post-amplifier and the envelope detector (both in Figure 10) are both disabled. When $V_{control}$ changes to 1.8 V, it starts to flow current from drain to sources of the transistors M_{1a} and M_{1b}, as well as in the transistors, M_{4a}, M_{4b}, M_{1c} and M_{1d}. In this last case, the currents drained from the *Bias* 2 and *Bias* 3 makes the post-amplifier and the envelope detector to be activated.

When this circuit is activated, the currents flowing in the *Bias* 1, *Bias* 2 and *Bias* 3 are 26 μA, 16 μA and 30 μA, respectively. Finally, the external resistor R_2 is responsible to impose the three former biasing currents, when the current that flows across it is 20 μA.

2.4 Transmitter

Figure 11 shows the block diagram of the transmitter, where a preliminary version of a digital

Figure 12. The schematic of the transmitter



ASK signal is generated in the modulator circuit, which combines the bitstream to be transmitted with the 2.4 GHz carrier. Then, this signal enters in an external filter, followed by a switched Power Amplifier (PA), whose output is the modulated ASK signal at the input of the antenna. The 2.4 GHz carrier is generated by a local oscillator, which is a Phase-Locked Loop (PLL) with an integer divider in the feedback path.

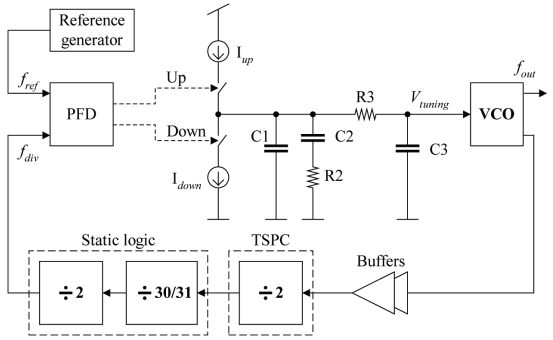
The power amplifier has a cascade of five inverter, in order to drive the digital ASK signal to the input of the power amplifier. Figure 12 shows the schematic of the whole transmitter, where it can be seen the modulator circuit, the power amplifier, the configuration used in the external filter and the power select circuit. In the last circuit it is possible to select the transmitted power. The Table 2 lists the several possibilities of transmitted power, the digital signals that select which power is to be transmitted.

Taking as an example, the situation where the logic states of the inputs *Power_select_1* and *Power_select_2* are "10", respectively, which put the transistor M_{17} in the conduction and maintaining M_{14} in the cut-off state. Thus, the base-idea is to inject a current I_{out} thru M_{15}, during a time corresponding to an half period of carrier and to remove the current I_{in} from M_{16}, during the remain

Table 2. Powers at the PA

Selection bits	Power consumption of the transmitter [mW]	Power consumption of Power Amplifier [mW]	Transmitted power [mW]
0 0			
0 1	10.67	4.97	0.28
1 0	12.62	6.91	1.01
1 1	13.61	8.02	1.21

Figure 13. The structure of the PLL



half of period. The wave for the current can be expanded in Fourier series as:

$$i(t) = \begin{cases} I_{out} & ,0 < t < \dfrac{1}{2f_C} \\ I_{in} & ,\dfrac{1}{2f_C} < t < \dfrac{1}{f_C} \end{cases} = \sum_{k=0}^{+\infty} i_k \cos(2\pi k f_C + \phi_k) \tag{8}$$

The network L_1-C_1 is tuned to the carrier frequency, while the emissions outside the 2.4 GHz band are reduced by the network L_2-C_2,, specially the strong second harmonic of the carrier, which were not sufficiently reduced by the network L_1-C_1. The peak power in an antenna with impedance of 50 Ω is:

$$p_{pk} = 10v_1^2 \text{ [mW]} \tag{9}$$

where v_1 is the amplitude [V] of the fundamental harmonic of the 2.4 GHz carrier in the antenna.

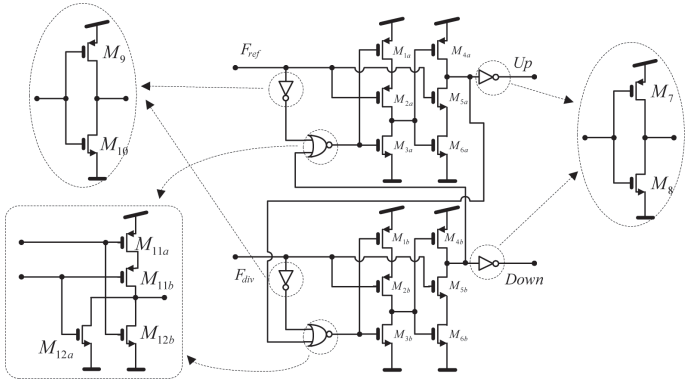
2.5 Frequency Synthesiser

The 2.4 GHz frequency carrier, is generated by means of a local oscillator, which is a Phase-Locked Loop (PLL). As depicted in Figure 13 the PLL has a reference generator circuit with a crystal based oscillator at 20 MHz (the value of f_{ref} [Hz]), followed by a phase-frequency difference circuit (PFD) without dead zone, a current steering charge pump (CP) and a third order passive filter (Carmo, 2007). The passive section output is connected to the VCO, whose output is the desired frequency of 2.4 GHz. This frequency must be divided by 120 (the division ratio, *N*, at the feedback path) and connected to the PFD again, closing the loop. In a PLL the frequency of the signal at the output is:

$$f_{out} = N.f_{ref} \tag{10}$$

In conventional PFDs there is an offset around the zero phase difference, and a gain inversion region takes place for phase differences higher than 2π-Δ rad. In this gain inversion region, the PFD outputs the wrong control signals increasing the phase and frequency differences between the inputs, and the lock

Figure 14. The schematic of the PFD



time takes a sudden turn for the worse (Lee *et al*., 2003). The implemented PFD has a linear gain in the range -π to +π, and a large constant gain in the range [-2π, -π] and [+π, +2π] (Kim & Kim, 2005). This type of PFDs makes PLLs faster, compared to those using conventional PFDs. Figure 14 shows the schematic of the implemented PFD.

The implemented CP is a current steering type (Figure 15). This circuit avoids the conventional problem in CPs, that limits the opening and closing of current sources, in fact, in spite of being switched, the current is routing from the load to an alternative path, and from that path to the load (Lin, 2000). When the control signal, $V_{control}$, is 1.8 V, the CP has a total power consumption of 1.04

Figure 15. The schematic of the implemented charge-pump

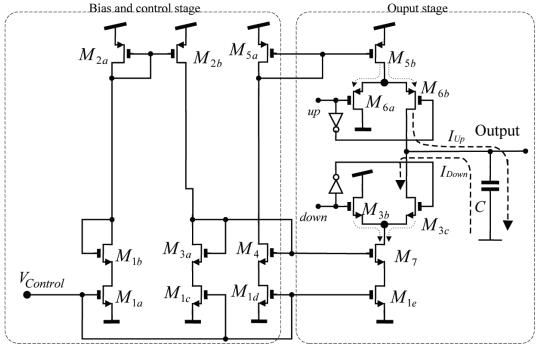
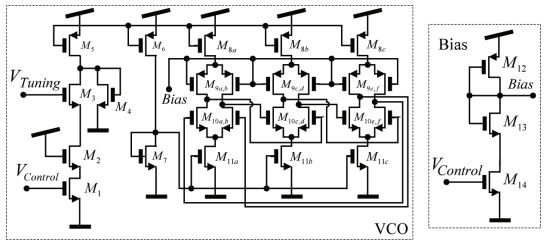


Figure 16. The schematics of VCO and bias



mW. The currents I_{up} and I_{down} are 173 µA and 178 µA, respectively, making the detector constant gain of the CP equal to K_φ=175 µA/2π rad.

The circuit shown in Figure 16, is a current starved ring oscillator and it was used as voltage controlled oscillator (VCO) in the differential configuration. Its operation is similar to ring oscillators. Transistors M_9 and M_{10} operate as an inverter, while M_8 and M_{11} operate as current sources. The current sources, M_8 and M_{11}, limit the current available to the inverter. M_9 and M_{10}; in other words, the inverter is starved for current. The transistors M_6 and M_7 are mirrored in each inverter/current source stage (Baker *et al*., 1997). Basically, the signal V_{tuning} imposes changes in the currents of the inverters, making them faster of lower to switch, e.g., it changes the propagation delays, τ [s]. Thus, for a N inverters VCO, the frequency of oscillation, f_{osc} [Hz], will be:

$$f_{osc} = 1/(N.\tau) = 1/[N.\tau(V_{tuning})] \quad (13)$$

Additional changes were made to the VCO presented in (Baker *et al*., 1997). It was added the transistors M_7, and M_{10}. The transistor M_7 controls the whole VCO, e.g., it uses the control signal, $V_{control}$, to enable and disable the VCO. The transistor M_4 allows to keep the oscillations at the VCO, when the voltage at the gate of the transistor M_3, V_{tuning} [V], falls below its threshold voltage, V_{thn} [V] (Morais, 2004). This makes possible to control the VCO at the full range [0, 1.8 V] for the voltage V_{tuning}. When active, the VCO has a power consumption of 2 mW.

Ring oscillators have more phase noise than *LC* oscillators. For overcoming this limitation, the bandwidth of the PLL must be high enough to "clean-up" the output spectrum around 2.4 GHz.

The division by 120 in the feedback path is done with a cascade constituted by one half divider implemented with a true single phase clock (TSPC) logic (Pellerano *et al*., 2004), one divider by 30, followed by a toggle flip-flop to ensure a duty-cycle of 50% at the PFD input. The TSPC logic was used to overcome the impossibility to implement the first toggle flip-flop with static logic in this technology. It is required a rail-to-rail input to work properly. The ratio of 30 was achieved with the use of simple frequency dividers by 2/3 with modulus control.

A third order passive filter, composed by a second order section (C_1, C_2 and R_2) and a first order section (C_3 and R_3), providing an additional pole it is used. The first order filter reduces spurs caused by the multiples of reference frequency, whose consequence is the increasing of the phase noise at the output. The stability is guaranteed by putting this last pole five times above the PLL bandwidth and below the reference. A bandwidth of approximately two times the difference between the maximum and minimum frequencies gener-

Figure 17. Behaviour of tuning voltage of the VCO, V_{tuning} [V]

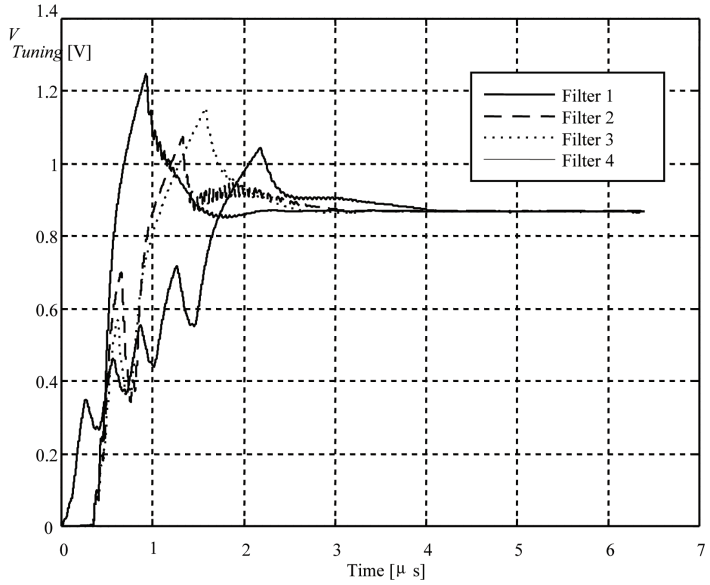
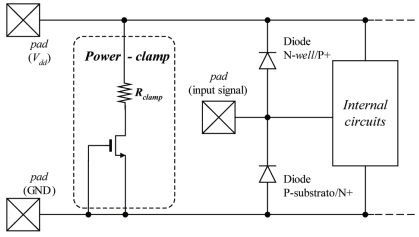


Table 3. Specifications, loop-filter components and the most significant results

Parameters	Filter 1	Filter 2	Filter 3	Filter 4
Phase margin - φ_p [º]	45	55	45	45
Bandwidth – f_p [MHz]	1.2	1.2	1.2	0.8
Frequency f_c [MHz]	0.82	0.75	0.64	0.51
Attenuation *attn* [dB]	10	10	15	15
C_1 [pF]	10	11.7	18	35
C_2 [pF]	81	180	185	300
R_2 [$k\Omega$]	5	3.7	3.5	2.7
C_3 [pF]	1	1	1.5	3.5
R_3 [$k\Omega$]	20	20	17.5	11
Time to converge [μs]	1.60	2.94	2.55	10.40
Actual phase margin [º]	44.8	55.3	49.1	45.6
Dumping - ξ	0.76	0.86	0.81	0.79

Figure 18. Protections against ESD discharges



ated by the VCO was used. The stability in the loop is obtained with a phase margin of at least $\pi/4$ rad (Gardner, 1980). The passive components were chosen with the help of a *template* for the *mathCAD* software (Ker & Lo, 2003) and the Table III shows some specifications, loop-filter components and the most significant results.

For the filters listed in the Table 3, the Figure 17 shows the temporal behaviour of VCO's tuning voltage, V_{tuning} [V].

2.6 Antenna Switch

An internal antenna-switch makes this transceiver a true complete system-on-a-chip (SOC). The antenna-switch connects the antenna to one of the receiver or transmitter path, that are connected to the receiving and transmitting ports, respectively. The isolation between non-connected ports must be high. In order to have a power efficient transceiver without degrading its sensitivity, the losses in the switch must be low.

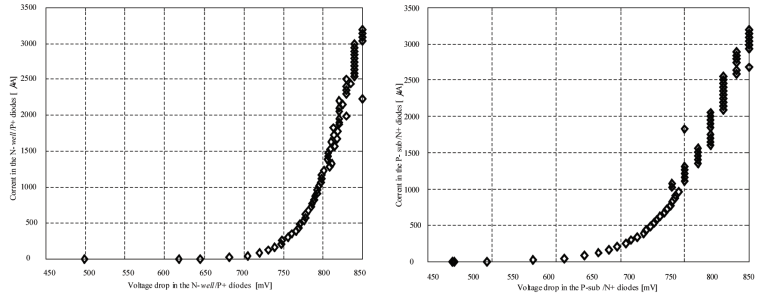
2.7 ESD Protections

The bondingpads are fundamental elements of an integrated circuit, e.g., they are used to connect the die to the external circuits and/or PCBs. Normally, during the chip design, it is necessary to prevent two effects that can arise: the first of them, is the latch-up. This effect can change the behaviour of the circuit, as well as to destroy it (Ker & Lo, 2003). Another effect, is the Electrostatic Discharge (ESD) on the die, which can cause its destruction (Vinson & Liou, 1998). The state-of-art shown, that ESD induced parasitics have been tolerated by regular ICs and, hence, have been largely ignored by IC designers in practices, they are becoming real limiting factors in RF and high-speed applications (Feng *et al*., 2004).

In the CMOS technology, the ESD destruction is a major concern. The destruction happens, because high currents are established, due to the breakdown of the dielectrics, where the silicon-oxides separating the gates of MOSFETs, from the channels, are an example (Ker *et al*., 2002). The resulting currents can be high and melt the surface of the die, leading the circuit to the total destruction. During the design and fabrication of the RF CMOS transceiver, it was considered two levels of protections (Ker *et al*., 1999; Ker *et al*., 2005): the first is the protection of the circuits, that connects to the bondingpads. The second level avoids the destruction of the internal circuits, from discharges coming from one of the two supply-rails (Figure 18). This level of protection is achieved by way of a power clamp, e.g., a transistor of N-type with its gate connected to the ground.

For the protection diodes, it's easy to get from its I/V characteristics, the serial resistance (R_d) and its threshold conducting voltage (V_{th}). This is made, applying a linear fit over that character-

Figure 19. I/V characteristics (a) for the N-well/P+ diodes, and (b) for the P-substrate/N+ diodes



a) b)

istics. Table IV shows the fitting results applied to the obtained I/V characteristics and shown in the Figure 19.

The quantification of the capacitance associated to the ESD protections is of major interest. The value of a capacitance, for a PN junction is given by:

$$C_j = \frac{C_{j0}}{(1+\frac{V_d}{\varphi_0})^m} \quad (14)$$

where, V_d is the DC reverse voltage bias, applied to the PN junction. C_{j0} is the junction capacitance with V_d=0 V, and φ_0 is the potential value of the junction. The capacitance of the diodes used as ESD protections, are given by:

$$C = \frac{C_j A_d}{(1+\frac{V_d}{\varphi_0})^{m_j}} + \frac{C_{jsw} P_d}{(1+\frac{V_d}{\varphi_0})^{m_{jsw}}} \quad (15)$$

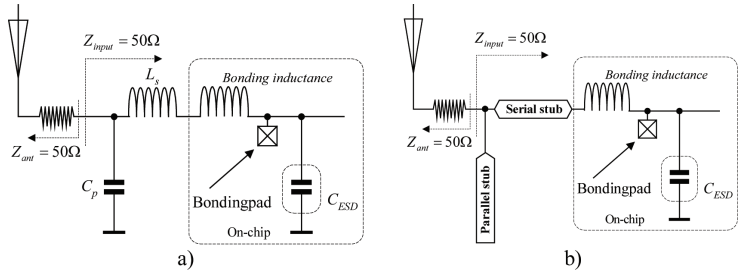
where A_d and P_d, are the area and the perimeter of the ESD protection diodes.

The used SPICE parameters are C_j=0.00119, C_{jsw}=1.6×10^{-10}, φ_0=0.79, m_j=0.515, m_{jsw}=0.381, for a area of A_d=675μm^2 (UMC 2001). Sweeping V_d in the voltage range [0, 1.8 V], it was obtained the worse value for the ESD capacitance. The former value is given by the sum of the capacitances, obtained for the two ESD protection diodes ($C_{nwell/P+}$ and $C_{psub/N+}$), which results equal to $C \approx$1.57 pF. Due to this parasitical capacitor, the input of the LNA is no longer matched with the antenna. This increases the return loss at the input, making the range smaller, for the same power transmission. Calculations shown a decrease in the range, from

Table 4. The serial resistance (R_d) and the threshold conducting voltage (V_{th}) of the ESD protection diodes

	P-substrate/N+ diodes	*N*-well/P+ diodes
R_d (Ω)	25.9	25.9
V_{th} (mV)	767.2	767.2

Figure 20. The simulated setups for the compensation of the ESD capacitance: a) with lumped circuit-elements, and b) with transmission lines, as circuit elements



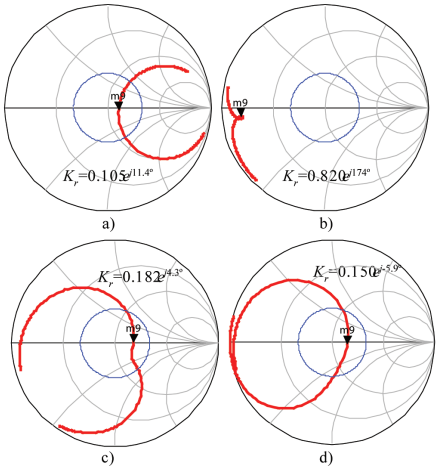
10 meters to 5.5 meters. Alternatively, for the same 10 meters range, the transmitted power must be 2 mW, in order to compensate the unexpected 3 dB losses (Table 4).

The solution to overcome the undesired effects, is the use of external elements (lumped or distributed), in order to have again, a perfect match between the input of the LNA and the antenna. The Figure 20 shows two solutions, to improve the behaviour of the circuit. The first setup is constituted by a classical matching network, which consists on a series inductance, L_s=1.5nH and a parallel capacitor, C_p=3pF. The second setup uses a series-stub (with characteristic impedance of 40 Ω and an electrical length of 30º) and a open-circuited parallel-stub (with characteristic impedance of 55 Ω and an electrical length of 69º). For the both setups, it was accounted the inductance of the bonding connection to the external PCB, which again, has been calculated to be 0.9 nH/mm (Alimenti *et al*., 2001).

Figure 21, shows four situations for the reflection coefficient (k_R) at the input of the LNA: a) ideally, without the effect of the ESD protections; b) with the effect of the ESD protections; c) with a compensation (matching) network made of lumped elements, and d) with a compensation network made of transmission lines (Carmo *et al*., 2008). It can be seen, that in the matching situation, the reflections decreases to acceptable values, e.g., the reflection coefficient, k_R is very close the centre of the Smith's chart. Solutions relaying on transmission lines are worthable than those using lumped elements, because it is achieved a better repeatability, due to the usage of lithography processes in the fabrication (Pozar, 2004). Moreover, a laser trimming technique can be used, when it is desirable a fine tuning of transmission lines.

A power-clamp is a transistor of N-type with the gate and source connected to the ground and with its drain connected to the Vdd (1.8 V) supply-rail, thus this transistor is normally in the cut-off state (Europractice, 2005). When the power-supply rises above acceptable values, the transistor enters in the conduction state, thus the impedance between the supply-rails will be low, compared with the rest of the circuit in the microdevice. In the case of the RF CMOS transceiver presented in this chapter, it was designed a set of power-clamps, one for each of circuit in the microdevice, e.g., for the RF, for the digital and for the analog circuits. The designed configuration uses a serial resistance to limit the discharge currents, in order to prevent the destruction of the microdevice by the power-clamp. The implantation of a supplementary layer in the zone of drain, helps to make the ESD protections more effective and themselves

Figure 21. Reflection coefficient (k_R) a) ideally, without the effect of the ESD protections; b) with the effect of the ESD protections; c) with compensation network formed by lumped elements, and d) with a compensation network formed by transmission lines



more robust to discharge currents (Ker *et al*, 2005; Ker *et al*, 2003; UMC, 2005). The widths of the N-type transistors must be as high as possible, to have a better flow of discharge currents (Ker *et al*, 2005; Ker *et al*, 2003). This power-clamp is a parallel of four (#4) N-type transistors, whose individual ratios are W/L = 12.5/0.36 [µm/µm]. It was simulated in the Advanced Design System (ADS) package, the behaviour of a power-clamp, when subjected to a ESD voltage of 4 kV. The obtained results revealed to be promising, because it was obtained a maximum discharge current of 32 mA and a voltage between the drain and the source of the transistor below 35.4 V. This makes the dissipated power to be only 1.13 W. Moreover, the use of transistors with ratios W/L = 12.5/0.36 [µm/µm], decreases the parasitic capacitance between the drain and the source, with the consequence to have less interference with the radio-frequency signals.

2.8 Experimental Results

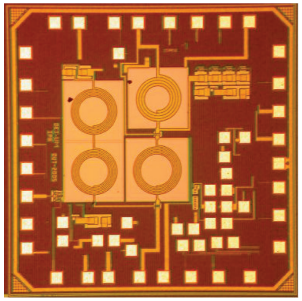
Figure 22 shows a photograph of the first prototype of a low-power/low-voltage RF CMOS transceiver, which has been fabricated in the UMC RF 0.18 µm CMOS process and occupies an area of 1.5×1.5 mm^2.

2.8.1 Setups Used in the Measurements

The experimental measurements were made with the help of two setups. In the first setup, it was used a probe station (model Karl Suss AP4). Figure 23 shows the test equipment, as well as a magnified photograph of the die and connection to the outside.

The second setup was made with the help of a wirebonding machine (model MEI 1204W). Fig. 24 shows a photograph of the wirebonding

Figure 22. A die photograph of the RF CMOS transceiver

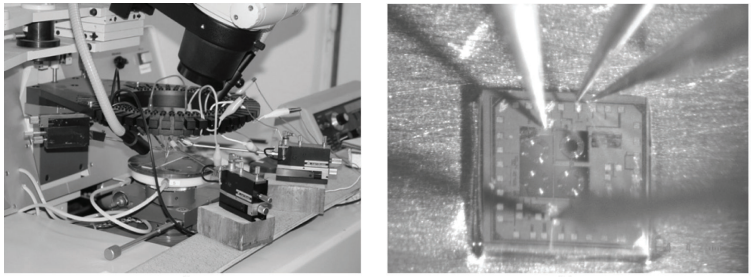


machine and the die. The second photograph also shows the connections between the bondingpads and the external PCB, which were made in Al-wires with a diameter of 20 µm.

2.8.2 Results

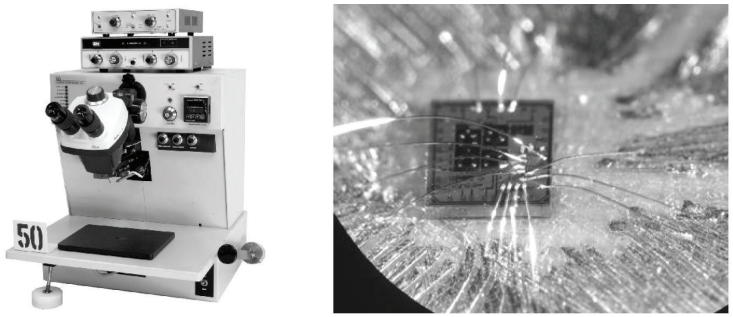
The experimental tests made to the RF CMOS transceiver, shown a total power consumption of 6.3 mW for the receiver (4 mW for the LNA, and 2.3 mW for the envelope detector and for the post-amplifier), and 11.2 mW for the transmitter. The transmitter delivers a maximum output power of 1.28 mW (very close to the specified 0 dBm) with a power consumption of 11.2 mW. When enabled, the power at the output of the PA, can be selected from the following values: 0.22 mW, 1.01 mW and 1.21 mW. It was observed for the LNA, a S_{21} of 19.2 dB, a noise figure (NF) of 3 dB, a 1 dB compression point (IP1) of -9 dBm, and a third order intercept point (IP3) of -5.4 dBm. The LNA has also a stabilisation factor of K=1.8 (greater than the unity), that makes this

Figure 23. (a) Photograph of the probe station used in the measurements; (b) a magnified view of the die



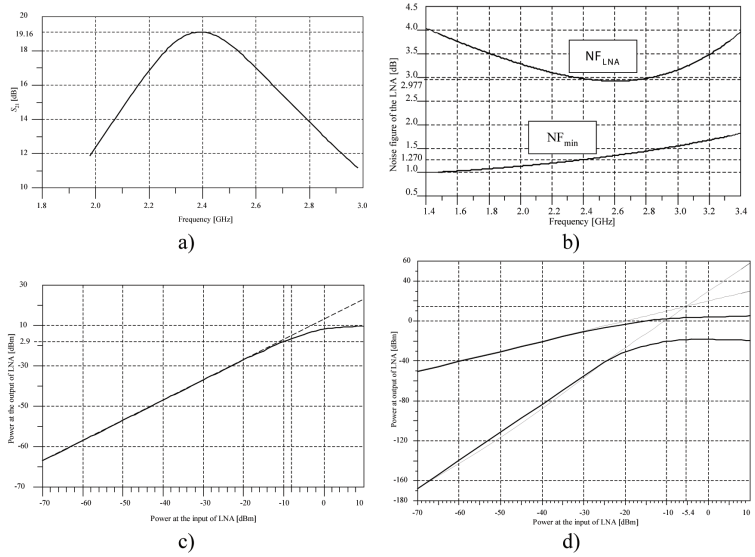
a) b)

Figure 24. (a) The wirebonding machine, and (b) a magnified view of the die, during the measurements



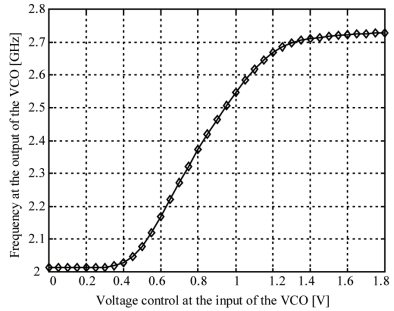
a) b)

Figure 25. For the LNA (a) the S_{21} [dB] parameter, (b) the NF [dB], (c) the 1 dB compression point (IP1) and (d) the third order intercept point (IP3)



a) b) c) d)

Figure 26. Measured working characteristic of the VCO



amplifier unconditionally stable. The Figure 25 shows the most important results.

The full range [0, 1.8 V] for the voltage V_{tuning} [V] shown in Figure 26, makes the VCO to oscillate in the frequency range of [2.02, 2.76 GHz]. A tuning constant of K_{VCO}=876.6 MHz/V was calculated in the linear working range of the VCO. As shown before, the judicious choosing of the loop-filter, allows to have for this PLL, the minimum time to lock of 1.6 μs (see Figure 17), e.g., less than half a bit duration time, at maximum baud-rate of 250 kbps. Finally, the antenna-switch provides a minimum port-isolation of 41.5 dB and a maximum insertion loss of 1.3 dB, overcoming the reference values in (Ugajin *et al*, 1997).

3 Biomedical Applications

Are many the applications for wireless microsystems with sensors, electronics of process and control, a RF transceiver and an associated antenna. The main idea is to acquire the values from sensors, store these values in the memory (if necessary) and relay it to an external base-station for further processing. Keeping this idea in mind, the focus of this section is the presentation of two biomedical applications for the fabricated RF CMOS transceiver are presented in this section. These applications are the wireless electroencephalogram (EEG) (Carmo *et al*, 2007) and an electronic shirt (e-shirt) for monitoring vital signals, such as the cardio-respiratory function (Carmo *et al*, 2008).

3.1 Wireless EEG

An emerging field is the wireless monitoring of human-body information. Body area network (BAN) comprises smart sensors able to communicate wirelessly to a base station. A wireless electroencephalogram (EEG) will provide a breakthrough in the monitoring, diagnostics and treatment of patients with neural diseases as epilepsy (Carmo *et al*, 2007). A wireless EEG module composed by the neural electrodes (non-invasive and distributed in a braincap), processing electronics and a RF transceiver with an associated antenna, will be an important breakthrough in EEG diagnostic (see Figure 27).

The RF transceiver (attached to an antenna) makes possible the data communication between the braincap and the external monitoring instrumentation used by health professionals. The RF transceiver must have low-power consumption, low-voltage supply and small-size so it can be

Figure 27. Classic EEG braincap with Ag/AgCl electrodes and respective wires

assembled with an antenna and the EEG electrode. The modules are feeded by a coin-sized battery placed in the braincap. The size-reduction achieved with these modules, make them suitable to be easily plugged and unplugged in the wireless EEG braincap according the interest of the medical doctors.

3.1.1 Electrode Concept

Recent advances in the biomedical field related with medicine and biology have been demanding more sophisticated electrode fabrication technologies (Patterson *et al*, 2004). Electrical activity occurs between neurons as well as in the muscles (e.g. heart) and nerves. The biopotential electrodes, jointly with acquisition systems, sense that electrical activity and make it accessible either for clinical or research trials.

Biopotential recording and excitable tissue stimulation have been accomplished by recurring to invasive and non-invasive electrodes. The neuroscience field has been demanding invasive electrodes that are implanted for single or multiple recording sites (Lebedev, 2006). Implanted electrodes are also used for deep brain stimulation (DBS) of neuronal ensembles and alleviate symptoms of Parkinson's disease. Non-invasive electrodes are used for biopotential recordings like electroencephalogram (EEG) (Griss, 2002), electrooculogram (EOG), electrocardiogram (ECG), electromyogram (EMG), among several other signals from the skin surface. Electrodes may also be employed on surface functional electrical stimulation (FES) (Mushahwar *et al*, 2007) and electrotactile stimulation (Kaczmarek *et al*, 1991). Electrotactile (also called electrocutaneous) stimulation is the activation of nerve fibbers within the skin with electrical current from surface electrodes thus generating sensations of pressure or vibration without the use of any mechanical actuator. Electrotactile stimulation can be used to convert visual information into tactile information (Kajimoto *et al*, 2004), augmenting or helping to rehabilitate subject's sensory perception.

3.1.2 Electrodes for EEG Systems

One of the keys to recording good EEG signals is the type of electrodes used. Electrodes that make the best contact with a subject's scalp and contain materials that most readily conduct EEG signals (low impedance), provide the best EEG recordings. Some of the types of electrodes available include:

1. **Reusable disks:** These electrodes can be placed close to the scalp, even in a region

with hair because they are small. A small amount of conducting gel needs to be used under each disk. The electrodes are held in place by a washable elastic head band. Disks made of Titanium, Silver, and Gold are available. They can be cleaned for example, with soap and water. The cost of each disk and lead is dependent on the type of metal used as a conductor, the gauge of wire used as a lead, and the type of insulation on the wire lead. Since these electrodes and leads can be used for years, their expense is low.

2. **EEG caps with disks:** Different styles of caps are available with different numbers and types of electrodes. Some caps are available for use with replaceable disks and leads. Gel is injected under each disk through a hole in the back of the disk. Since the disks on a region of the scalp covered with hair cannot be placed as close to the scalp as individual disc electrodes, a greater amount of conducting gel needs to be injected under each. After its use, more time is required to clean the cap and its electrodes, as well as the hair of the subject. Depending on the style and longevity of the cap and the electrodes, their expense can be moderate to high.
3. **Adhesive gel electrodes:** These are the same disposable silver/silver chloride electrodes used to record ECGs and EMGs, and they can be used with the same snap leads used for recording those signals. These electrodes are an inexpensive solution for recording from regions of the scalp without hair. They cannot be placed close to the scalp in regions with hair, since the adhesive pad around the electrode would attach to hair and not the scalp. When purchased in bulk, their expense is very low.

Beyond its electrical properties, another and not less important requirement for good electrodes, is the issue related to the biocompatibility. The best definition of biocompatibility, is the ability of a material to perform with an appropriate host response in a specific application, thus EEG electrodes must match this requirement. Following, it is shown a comparison of used electrodes, e.g., the Silver/Silver Cloride electrodes, the Sputtered Titanium Nitride electrodes and the Sputtered Iridium Oxide electrodes. Polarizable electrodes such as Stainless Steel and Platinum are not suitable for the application described on this paper, due to its non-effectiveness on the recording of EEG slow-potentials (Ikeda *et al*, 1998).

3.1.2.1 Silver/Silver Cloride

Standard sintered Ag/AgCl ring electrodes are frequently used for clinical and biomedical applications (e.g. electrocardiography and electroencephalography) and they usually present very low skin-contact impedances and reasonable stability over the required frequency range.

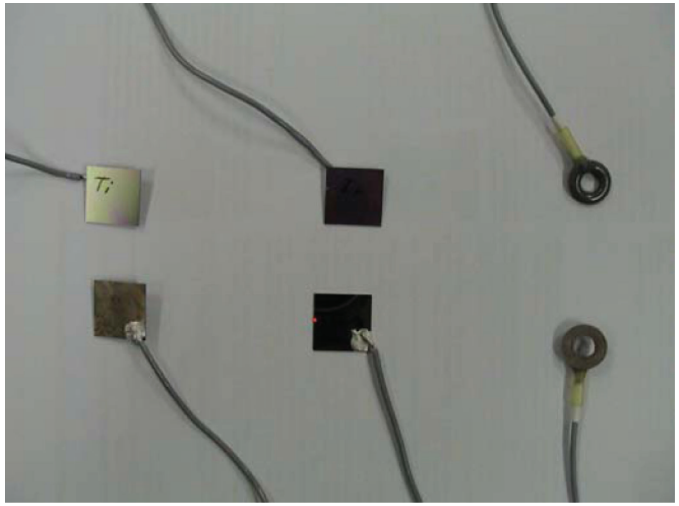
3.1.2.2 Sputtered Titanium Nitride Electrodes

TiN was deposited by means of DC magnetron sputter deposition from a Ti target in an Ar/N_2 plasma. A Nordiko NS 2550 sputtering equipment was used for TiN deposition and the sputtering chamber was evacuated to at least $4x10^{-6}$ mbar by means of a cryogenic pump. A previous study of the nitrogen gaz flow (between 0.6 sccm and 2.2 sccm) showed that for the same pumping speed (270 l/s) and a power of 500 W the lowest resistance is achieved with 0.8 sccm N_2 (440×10^{-6} Ω.cm at films with a thickness of 230 nm).

3.1.2.3 Sputtered Iridium Oxide Electrodes

Also IrO_2 was deposited by means of DC magnetron sputter deposition from a target in an Ar/O_2 plasma, prior to which a Ti adhesion layer (with a thickness of 50 nm) was deposited on the substrate. The oxygen gas flow was fixed at 1.85 sccm according to the procedure described in (Wessling *et al*, 2006). The IrO_2 resistance in

Figure 28. The fabricated/mounted electrodes in a set of pairs, from left to right, sputtered TiN electrodes, sputtered IrO_2 electrodes, and standard sintered Ag/AgCl ring electrodes (Correia et al, 2006)



a 270 nm thick film was 349×10^{-6} Ω.cm (Figure 28) (Correia *et al*, 2006). The thicknesse of films were determined via lift-off process with a Tencor Pa-10 profilometer. The thin film resistance was measured in a classic 4-point probe system.

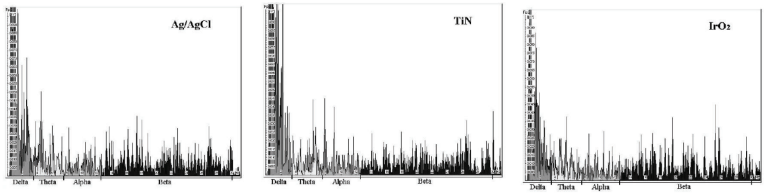
3.1.2.4 Electrodes Impedance Comparison

Electrode impedance reflects the electrode's capability to transfer signals at a given frequency. For the desired frequencies (up to 30 Hz), the standard Silver-Silver/Cloride and Titanium Nitride electrodes have typical contact resistances less than: 1-6 kΩ, 29-80 kΩ. The electrodes using traditional materials, such as the Stainless Steel, Platinum and Gold, the impedances are as following: for the Stainless Steel and Platinum, the impedance responses go almost immediately out of a maximum given scale of 120 kΩ, because of rapid polarization (shown schematically with the dashed line). The commercial Gold electrodes has a typical impedance of 50-92 kΩ. Gold electrodes presents very high values, compared with those found in the Silver/Silver-Chloride and Titanium Nitride electrodes, which are not higher than 1-6 kΩ, and 29-80 kΩ, respectively (Tallgren *et al*, 2005).

3.1.3 Comparison of EEG Electrodes

The amplitude of the EEG is about 70 μV when measured on the scalp. The bandwidth of this signal is from under 1 Hz to about 50 Hz. The data-acquisition system used in the experiments is composed of an amplifier with 40 channels, connected to analog-to-digital converters of 22-bits (sampling frequency at 2000 Hz), and a braincap with large filling holes and flat clip-on adapters making skin preparation and gel application

Figure 29. The FFT response in terms of power (μV^2) versus frequency for a) standard sintered Ag/AgCl ring electrodes, b) sputtered TiN electrodes, and c) the fabricated sputtered IrO_2 electrodes



a) b) c)

simpler, improving preparation time. The amplifier is connected to a PC (via USB) that runs the recording software. The recording electrode was applied in the frontopolar area (in position FP2) in a standard configuration 10-20 system used in EEG clinical diagnostics and the other electrode of the pair was the reference.

During the measurements the patients were in contemplation of a picture for trying to avoid the frequently blinking of the eyes during 3 minutes. The study contemplated the extraction of the power of the signal in FP2 versus the frequency, using the Fast Fourier Transform in the range of interest, 0.5-30 Hz, for EEG (analysing the Delta 0.5-3 Hz, Theta 3-7 Hz, Alpha 7-13 Hz and Beta 13-30 Hz waves). Figure 29 (a) to (c) show the FFT response of the standard sintered Ag/AgCl ring electrodes, sputtered TiN electrodes and sputtered IrO_2 electrodes, respectively.

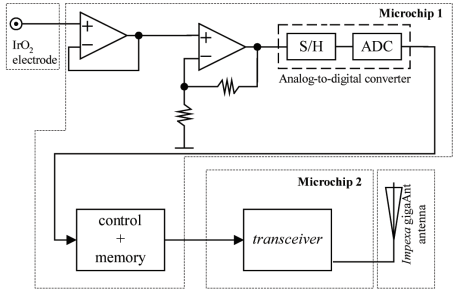
The FFT response was obtained in terms of power of the signal (μV^2) versus the frequency. The amplitude of the signal in average is higher for the IrO_2 electrodes (high-amplitude signals in subdelta). Also, they have an excellent response in Theta and Beta waves compared to the standard sintered Ag/AgCl ring electrodes. The sputtered TiN electrodes shows an excellent amplitude signal in Alpha waves but they show the lowest amplitude of the signal in average compared with the standard sintered Ag/AgCl ring electrodes and the sputtered IrO_2 electrodes. In (Heuvelman *et al*, 1998), sputtered TiN thin films deposited with a pumping speed of 9 l/s and a power of 2.2 kW, and nitrogen gas flow of 3.4 sccm showed a resistance in the range of $27\text{x}10^{-6}$ Ω.cm to $33\text{x}10^{-6}$ Ω.cm. Comparing with the sputtered TiN films resistance fabricated in this work, we believe that their performance as EEG electrodes will be improved.

The new direction in research by this emerging technology will soon require neural electrode arrays for stimulating and recording containing hundreds of electrodes. Following this tendency, the work reported in (Dias *et al*, 2008), describes the use of the characterized DC-sputtered IrO_2 to coat a fabricated electrode with micro-tips. These tips were micro-machined through a wet etching process with undercut in a KOH solution. The fabricated tips are about 100 μm high with a pyramidal shape in order to be able to pass through the outer skin layer, e.g., the stratum corneum.

3.1.4 Wireless EEG Modules

The standard wireless EEG solutions use a braincap with wires running from the electrodes position to a bulky central unity (amplification, signal filtering and analog-to-digital conversion, RF transceiver and antenna) (Carmo *et al*, 2007). A more interesting solution is to use compact wireless EEG modules, where the electronics, the antenna and each electrode are mounted together.

Figure 30. Wireless EEG module. Note that the neutral electrode, which is connected to the grounds of the module it is not shown.



The power supply for these modules is obtained locally from a coin-sized battery placed in the braincap.

Bipolar or unipolar electrodes can be used in the EEG measurement. In the first method the potential difference between a pair of electrodes is measured. In the second method, the potential of each electrode is compared, either to a neutral electrode or to the average of all electrodes. Figure 30 shows the full schematic of the wireless EEG module, where it can be seen the electrode connected to an amplifier, followed by an A-to-D converter. In order to meet the EEG specifications, the amplifier was designed to have enough gain, to amplify signals with amplitudes of only 70 μV. The analog-to-digital converter (ADC) was designed to have a resolution of 22 bits and a minimum sampling frequency of 2000 Hz. The electronics comprising the control logic and the memory was designed together with the amplifier and ADC in the same microchip.

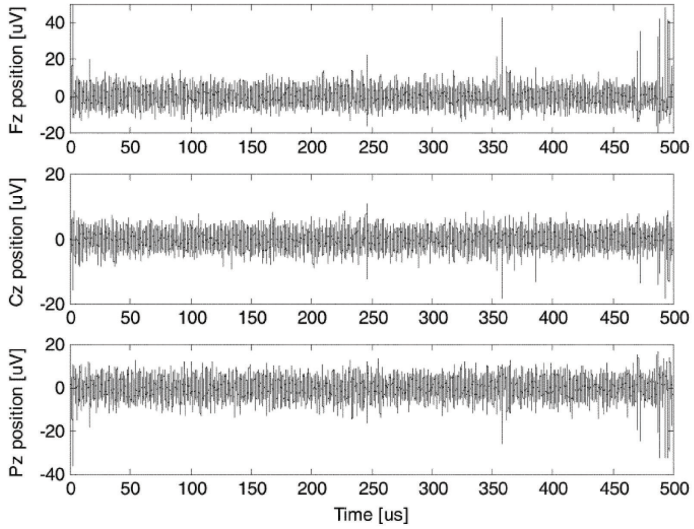
Figure 31 shows three simultaneous acquired (reconstructed) signals from three of the proposed wireless EEG modules. These signals were obtained during a period of 500 μs, from Fz, Cz, and Pz positions. The dynamic variation of the three EEG signals didn't exceed 70 μV.

The modules must offer the plug-and-play feature, in order to mount distributed networks in the patient's head. Moreover, as the EEG data is periodically acquired in all the modules, thus the latencies of data transmissions are not allowed. The proposed EEG modules uses a communication protocol that overcomes these problems (Afonso *et al*, 2006). This protocol combines the distributed and coordination modes, e.g., when a new module is putted in the head of patient, a contention based time interval is used to make the registration request in the network. A contention-less time interval, constituted by time-slots, is granted to the new EEG module if the registration is successful completed on the network. The maximum number of simultaneous modules is limited to the number of time-slots in the contention-free interval.

Figure 32 is a photograph of a full wireless EEG module, where it is shown the sputtered IrO_2 electrode mounted together with the processing and control electronics (is the microchip located above), the RF transceiver (is the microchip located below) and an associated antenna. The whole electronics and the associated antenna are mounted in the back of the electrode package.

This solution fits the medical doctor requirements for an easy placement and removal of the electrodes in the braincap. Moreover, with this

Figure 31. Reconstructed EEG signals, simultaneously acquired in the Fz, Cz and Pz positions



solution it is very easy to populate electrodes in different positions or takeoff. In many medical diagnostics the patients are monitorized only with a low number of electrodes (e.g. 2-5 electrodes), making possible to mount an EEG wireless-electrodes network with these plug-and-play modules.

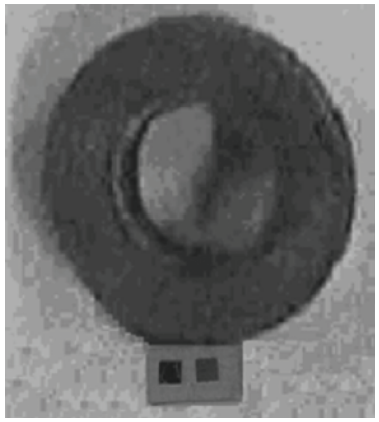
3.2 Smart Textiles

Today, the link between textiles and electronics is more realistic than ever. An emerging new field of research that combines the strengths and capabilities of electronics and textiles into one: electronic textiles, or e-textiles is opening new opportunities. E-textiles, also called smart fabrics, have not only wearable capabilities like any other garment, but also have local monitoring and computation, as well as wireless communication capabilities. Sensors and simple computational elements are embedded in e-textiles, as well as built into yarns, with the goal of gathering sensitive information, monitoring vital statistics, and sending them remotely (possibly over a wireless channel) for further processing (Marculescu *et al*, 2003). The goal of the Wireless Electronic Shirt (WES), is the monitoring of the cardio-respiratory function. This makes it able to recognise qualitatively and quantitatively the presence of respiratory disorders, both during wake and sleep-time in free-living patients with chronic heart failure, providing clinical and prognostic significance data.

3.2.1 The Wireless Electronic Shirt (WES)

Like any other every-day garment piece, the wireless electronic shirt (WES) will be lightweight,

Figure 32. A module photograph, where it is shown the sputtered IrO_2 electrode mounted together with the electronics (the microchip on the left), the RF transceiver (the microchip on the right) and a planar antenna

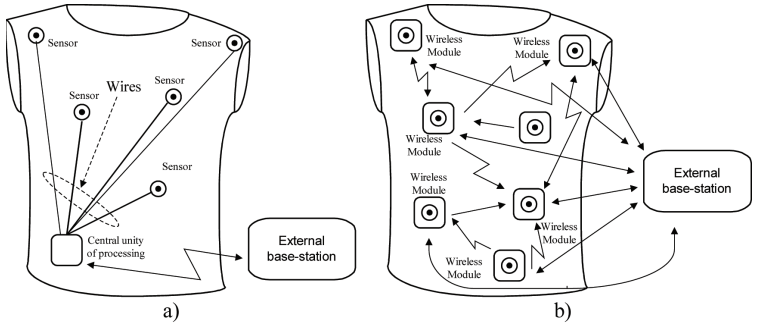


machine washable, comfortable, easy-to-use shirt with embedded sensors. To measure respiratory and cardiac functions, sensors are plugged into the shirt around patient's chest and abdomen. The WES also uses small sizes and compact modules, made with microsystems, containing the 2.4 GHz RF CMOS transceiver, the electronic of control and processing, and the interfaces to make the connections to the sensors. These modules have also an associated antenna and are supplied by a coin-sized battery. The size-reduction achieved with these modules, make them suitable to be easily plugged in the WES, according the interest of the medical doctors.

The Figure 33 (a) shows the communication scenarios found in conventional applications of electronic shirts. Generally, a flexible data bus integrated into the structure, is used to route the information from the sensors to the controller (Coosemans *et al*, 2005). Examples of such products includes the shirts found in (Edwards, 2006), which are used in remote life-signs monitoring systems for use by firefighters, police, industrial clean-up workers or others. Another non-flexible example of wearable is a system used to collect analog signals through conductive fiber sensors and passes them through a conductive fibre grid knitted in a shirt (Batista, 2001). In this shirt, a textile connector passes the analog signals to a small personal controller held in a pocket on the shirt, then the personal controller digitises the signal and transmits the signal to a *Bluetooth* or *Zigbee* receiver connected to a base-station where the information is further collected and analysed. The wired concept is a problem when the textiles going to wash, because require removal of complex electronics before starting the cleaning process. Another disadvantage, is that the topological location of different processing elements is fixed throughout the lifetime of the applications.

An interesting application and an easy way to implement wireless buses, is using modules able to communicate between them and between

Figure 33. (a) Conventional application, where wires are used to connect the sensors to a centrally located unity of processing, and (b) the wireless bus mounted in the proposed wireless electronic shirt



the base-station. As shown in the Fig. 33(b), this solution fits the medical doctor requirements for an easy placement and removal of the wireless modules in the shirt. Moreover, with this solution it is very easy to populate wireless modules in different positions or takeoff.

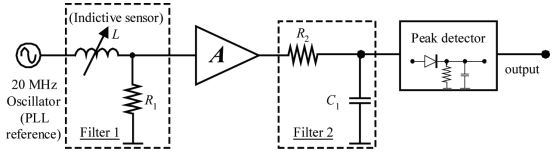
The modules must offer the plug-and-play feature, in order to mount distributed networks in the WES. Moreover, as the data is to be periodically acquired in all of the modules, thus the latencies of data transmissions are not allowed. The proposed wireless modules can also use the communication protocol described in (Afonso *et al*, 2006) to overcome these problems.

The target application for the WES, is the measure of the cardio-respiratory function, where a single channel measures heart rate and a MEMS capacitive accelerometers network records patient posture (arms and body position) and activity level (arms movements). Inductive cooper filaments will be used for monitoring the respiratory function. However and as discussed further. The WES and the wireless modules are not restricted to be used to measure the cardio-respiratory function.

A bending sensor can be used to monitor the shoulders positions. The sensor has changes in the electrical resistance when it is bent. An unflexed sensor has a nominal resistance of 10 kΩ and as the sensor is bent, the resistance gradually increases. When the sensor is bent at 90 degrees, its resistance will range between from 30 kΩ up to 40 kΩ (Image, 2009).

An elastic band can be used to measure the changes in thoracic circumference due to respiration. The transducer contains an variable inductance, used indirectly to measure the changes in thoracic circumference. The device should be placed around the body at the level of maximum respiratory expansion. This level will change between erect and supine positions. At maximum inspiration the belt should be stretched almost to maximum extension, making its inductance minimum. As shown in the Figure 34, the PLL reference oscillator is used to generate a 20 MHz sinusoidal signal. The variations in the inductance, changes the attenuation for the 20 MHz signal, in the first *RL* low-pass of first order filter. Thus, the attenuation increases with the decreasing of the thorax perimeter. This filtered signal is further amplified, before a second low-pass filtering, to eliminate noise and spurs generated in the 20 MHz oscillator. Then, a peak detector gets the amplitude of the 20 MHz processed signal. The peak voltage is:

Figure 34. The block diagram of a signal conditioning used in the measure of the respiratory function



$$V_{pk}(s) = \frac{V_{20}.A.R_1}{R_2 C} \times \frac{1}{s + \frac{1}{R_2 C}} \times \frac{1}{L} \times \frac{1}{s + \frac{R_1}{L}} \quad (16)$$

where, V_{20} [V] is the amplitude of the 20 MHz sinusoidal signal and A is the gain of an amplifier used to make the voltage at the output of the peak detector to cover the entire range of the further analog-to-digital converter (ADC) chain. This amplitude follows the low-frequency respiration signal and it is converted to the digital domain, using an ADC with an output resolution of 8 bits.

In WES, the sensor interfaces, data processing, the wireless interface and antenna are integrated in the same microsystem by multi-chip-module (MCM) techniques. The wireless communication is between the base-station and the multiple processing elements placed in the shirt. The main advantage is to allow the positioning of the sensors where we like. The sensors can also be removed from the shirt, either when the sensors are no more need or when the shirt is to be cleaned and washed. This wireless bus introduces the concept of plug-and-play in textiles.

As shown in Figure 35, each microsystem can be connected to up two external sensors, by way of each interface. The electronics of control the read operation between one of the interfaces and routes the signal from the respective sensor read-out, across an analog multiplex. Then if necessary, additional amplification is possible to be made on-chip. An internal ADC makes the conversion of the amplified signal to the digital domain. Finally and in order to provide some autonomy working, the acquired values from the sensors must be temporary stored in the internal memory.

It is shown in Figure 36, a photograph of a patient wearing an WES ready to plug the RF

Figure 35. The block diagram of the microsystems used in the plug-and-play modules of the WES

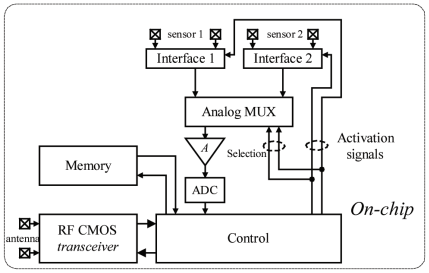


Figure 36. A photo of the patient wearing a electronic shirt ready to plug the RF modules

modules. It can be seen three connections for heart-rate respiratory function.

An additional advantage of the wireless acquisition modules composed by these microsystems, is the reusability, e.g., the monitoring of the cardio-respiratory function is not the only possible application. Indeed, another applications of sensors in WES are possible.

4 FUTURE TRENDS

The future of RF microsystems pass with the use of MEMS (Micro Electro Mechanical Systems) based components (Nguyen *et al*, 1998). An example of such a component can be the generator of the reference frequency used in the PLL. Crystal-based piezoelectric oscillators normally require a huge areas, compared with those used by the associated electronics (when they exist, the inductances and capacitors are not included in this set), thus an additional space must be provided in the PCB (Printed Circuit Board) with the inevitable consequence of an increase in the total production cost. Moreover, the accuracy and the stability of the produced frequency by these oscillators are temperature dependant and the error will be multiplied by the PLL, e.g., if the actual reference frequency is $f_{ref2}=f_{ref}\times(1\pm\Delta f)$, the actual carrier frequency will be:

$$f_{out2} = N.f_{ref2} = N.f_{ref} \pm N.f_{ref}.\Delta f = f_{out} \pm \Delta f_{out} \quad (17)$$

where N is the division ratio of a PLL, f_{ref} [Hz] is the error-free reference frequency of a PLL, $\pm\Delta f$ [Hz] is the drift (above or below) in the reference frequency, f_{out} [Hz] is the error-free carrier frequency. A special concern must be taken in account, specially for high division ratios, N, and high reference frequencies, f_{ref} [Hz], in the PLL, because the overall drift (or propagated error) in the frequency at the output of the PLL, $\Delta f_{out} = N.f_{ref}.\Delta f$ [Hz], can be critical.

Beyond the advantage to have a small area occupancy, MEMS resonators allows to make an accurate trimming in the frequency of oscillation. Moreover, the simple matter of fact this adjustment could be made in an electrically form constitutes an inexorable advantage over the Crystal oscillators (Yao, 2000).

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KEY TERMS AND DEFINITIONS

Biomedical Applications: Activities of science applied to the clinical medicine.

Cardio-Respiratory Function Monitoring: Monitoring of the breath rate at the same time, cardiovascular signals are being acquired.

CMOS: Complementary metal oxide semiconductor.

Microsystem: System comprising active and passive components of various technologies that were assembled in the same die, by a mounting process.

RF Transceiver: Electronic system responsible to transmit and receive electrical signals in a reliable form;

Wireless EEG: EEG whose acquired signals are transmitted by radio frequency.

Wireless Sensor Networks: A network comprising wireless nodes, whose principal function is to acquire physical measures and send them wirelessly towards a base station. Also, these nodes can work as relays to other nodes or directly to the base station, and it must possess the ability to temporarily store its acquired data and the data to be forwarded.